Hardware Operators for Pairing-Based Cryptography

— Part I: Because size matters —

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Nicolas Estibals	CACAO, LORIA, Nancy, France
Eiji Okamoto	LCIS, University of Tsukuba, Japan
Francisco Rodríguez-Henríquez	CSD, IPN, Mexico City, Mexico

Outline of the talk

- Pairing-based cryptography
- Pairings over elliptic curves
- Finite-field arithmetic
- Implementation results
- Concluding thoughts

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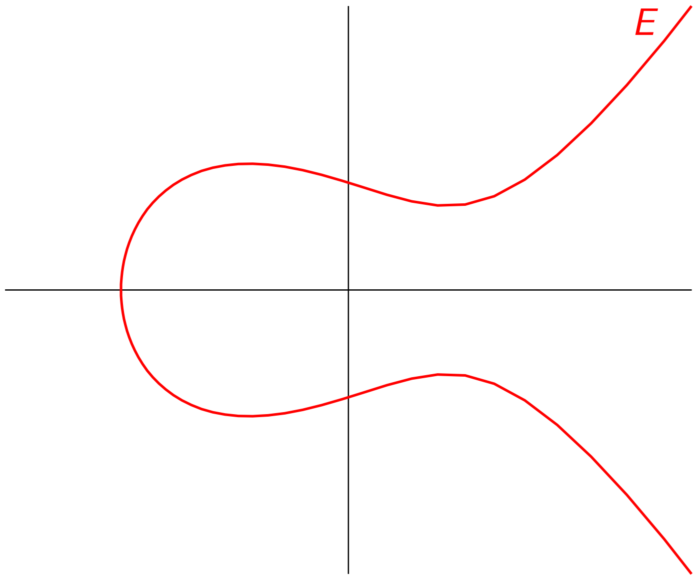

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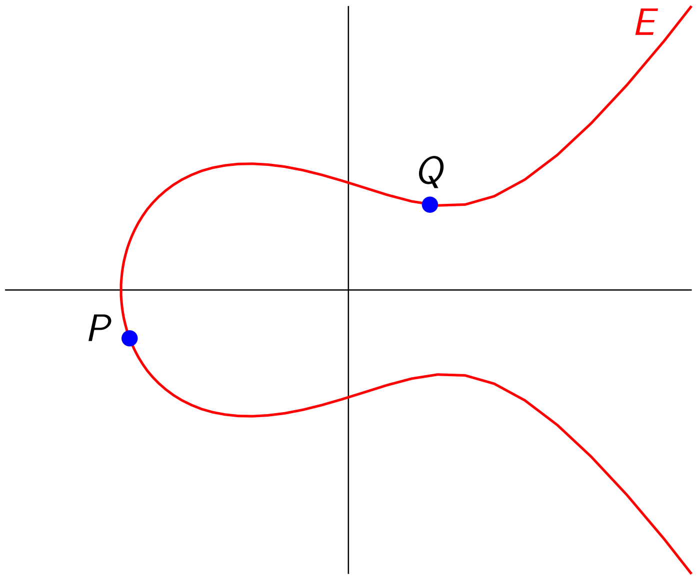

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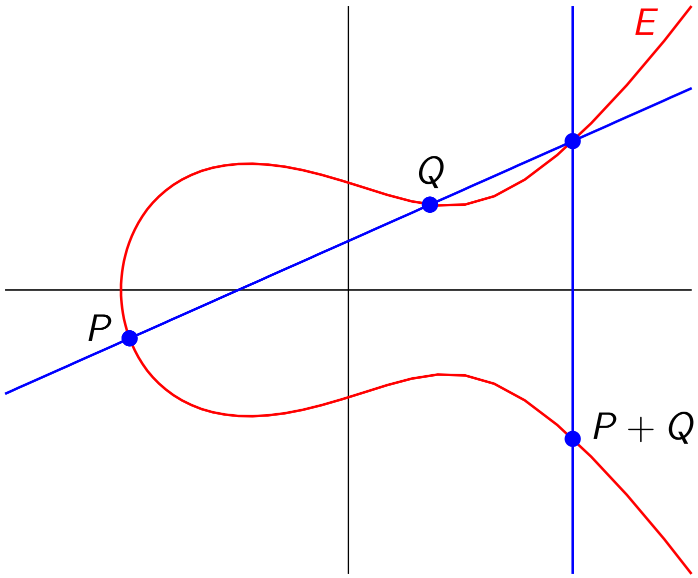

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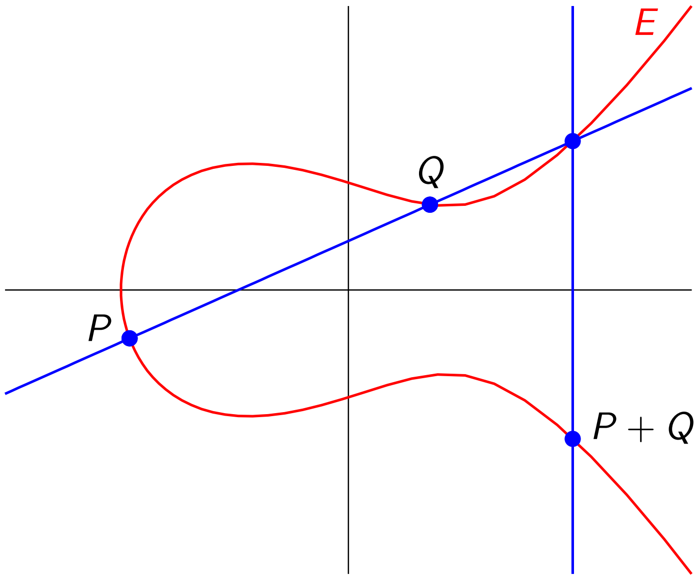

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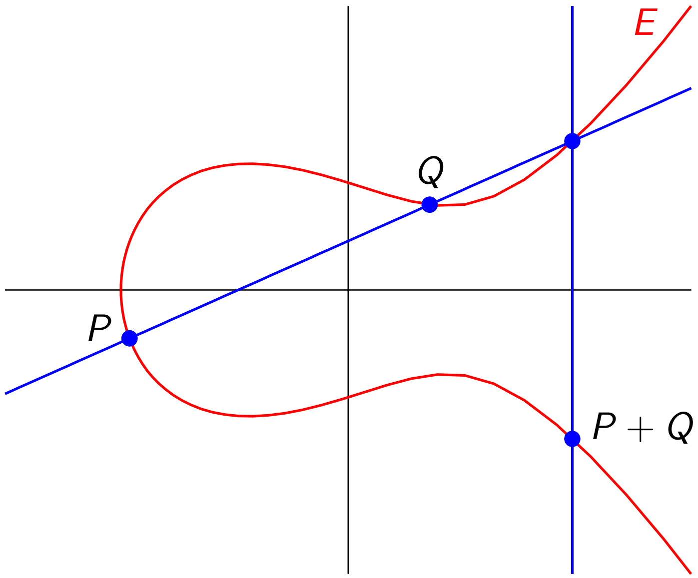
- But there's more: bilinear pairings



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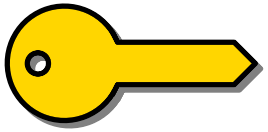

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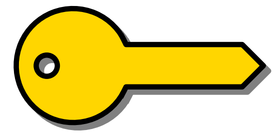

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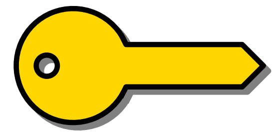

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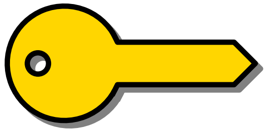

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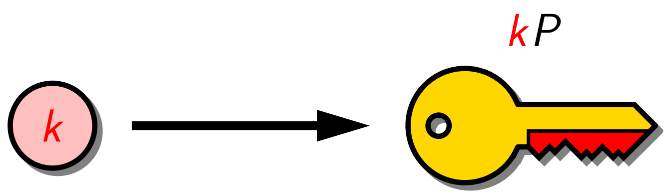

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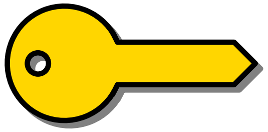

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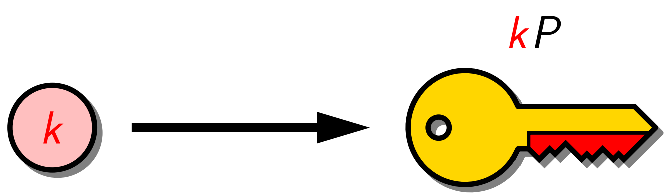

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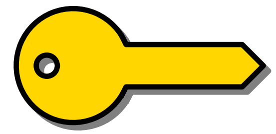

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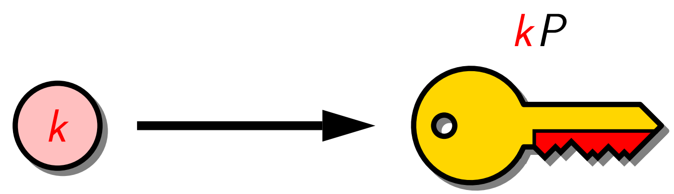

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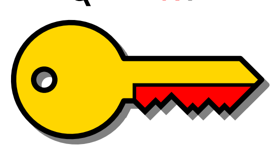

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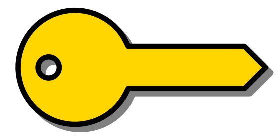

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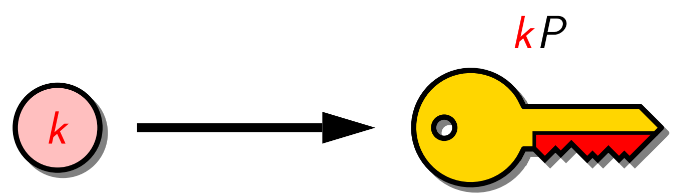

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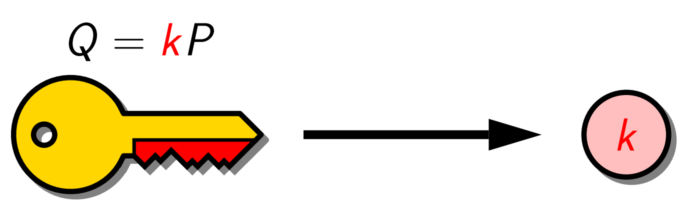

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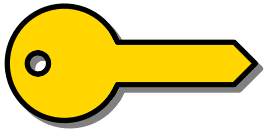
- P, a generator of the group: $\mathbb{G}_1 = \langle P \rangle$ 
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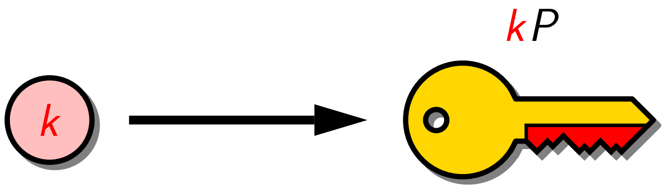

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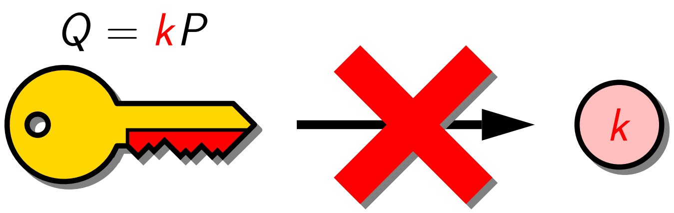

- We assume that the discrete logarithm problem (DLP) in $\mathbb{G}_1$ is hard

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  that satisfies the following conditions:

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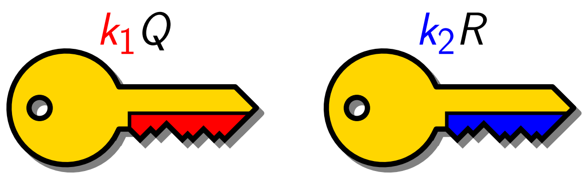

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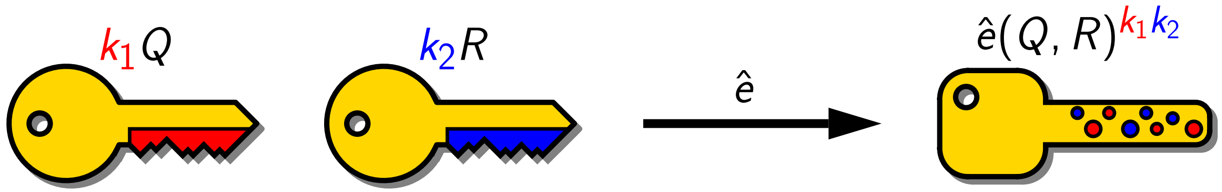

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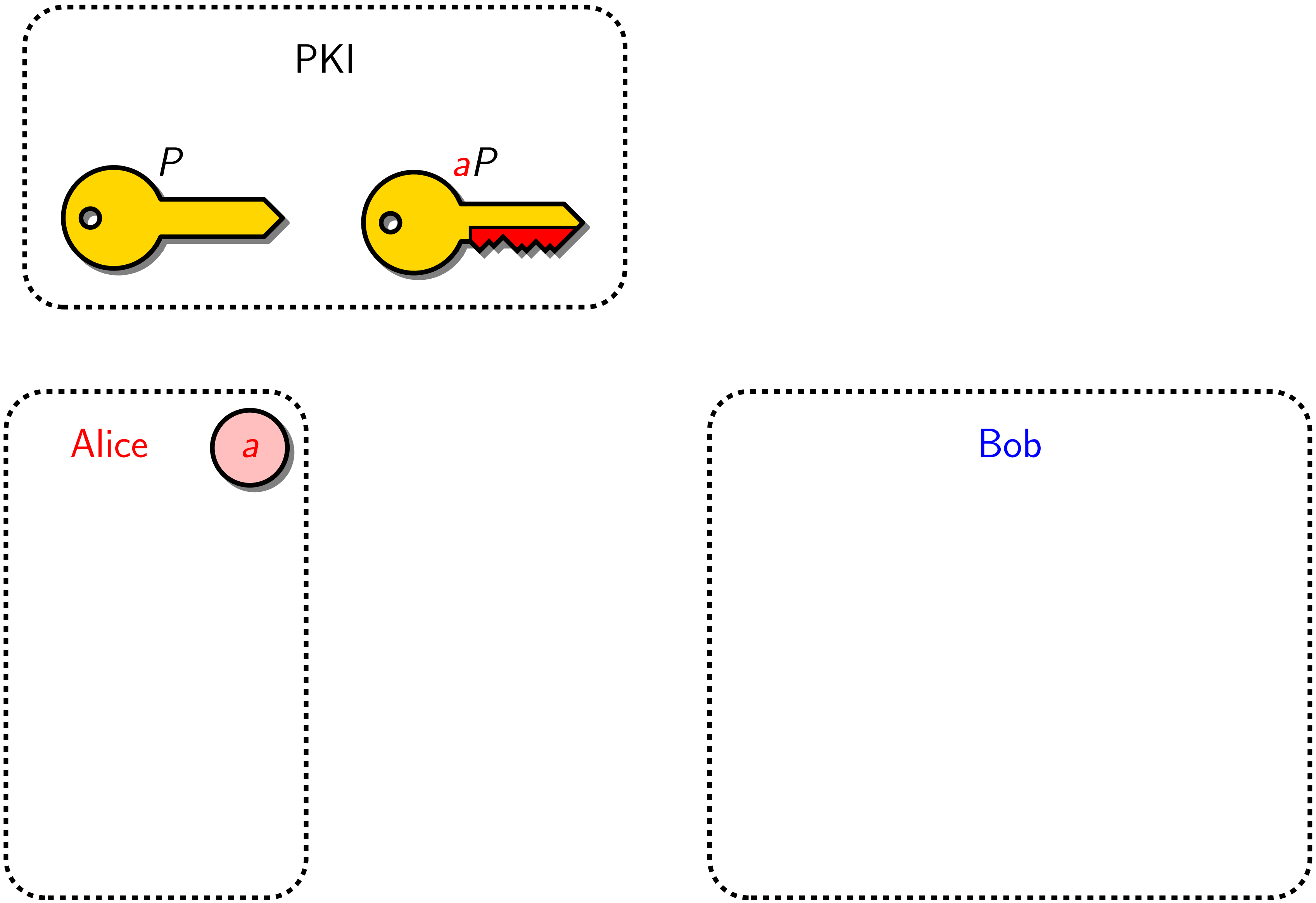
- One-round three-party key agreement (Joux, 2000)
- Identity-based encryption
  - Boneh-Franklin, 2001
  - Sakai-Kasahara, 2001
- Short digital signatures
  - Boneh-Lynn-Shacham, 2001
  - Zang-Safavi-Naini-Susilo, 2004
- ...

Short signature (Boneh, Lynn & Shacham, 2001)



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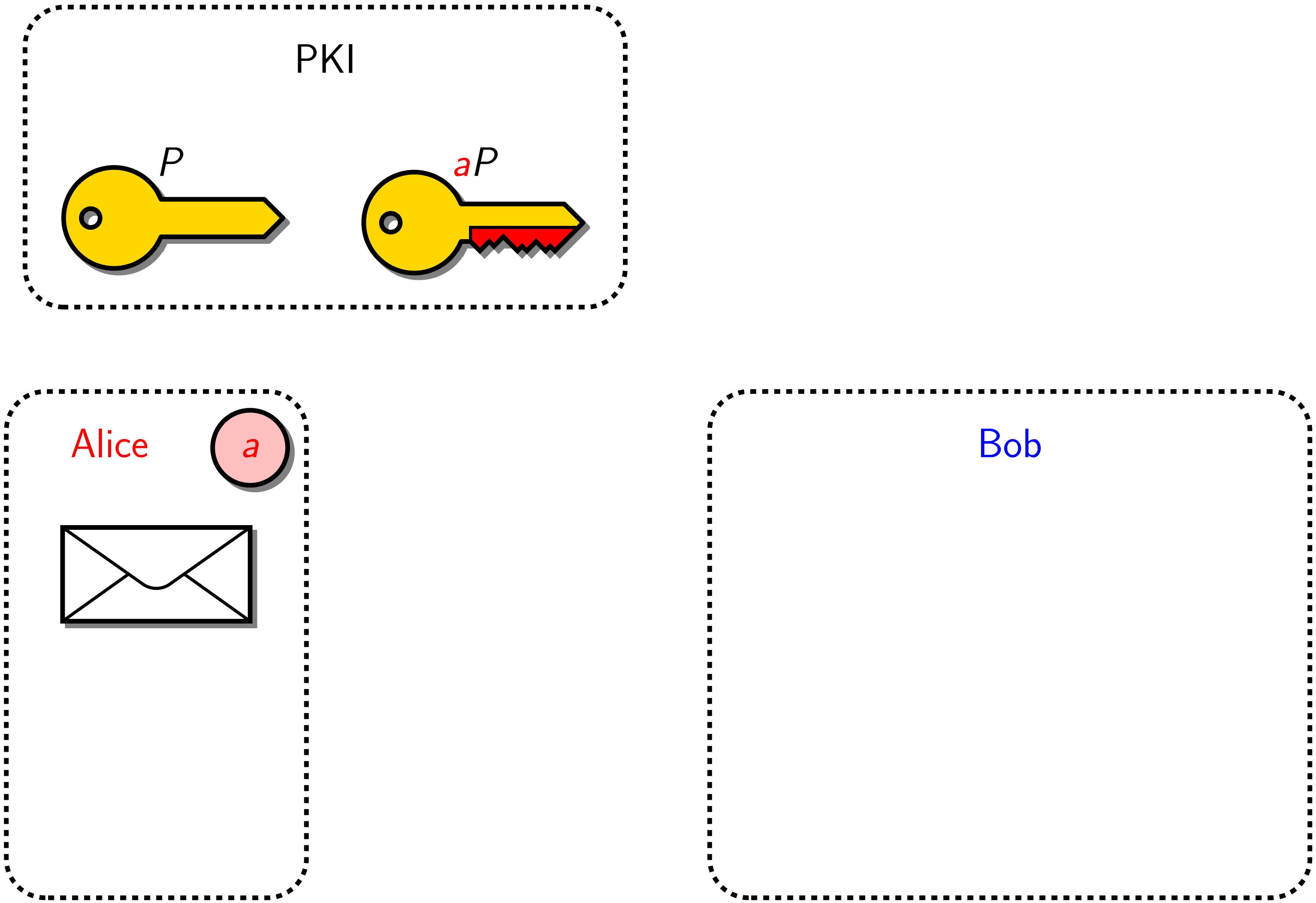

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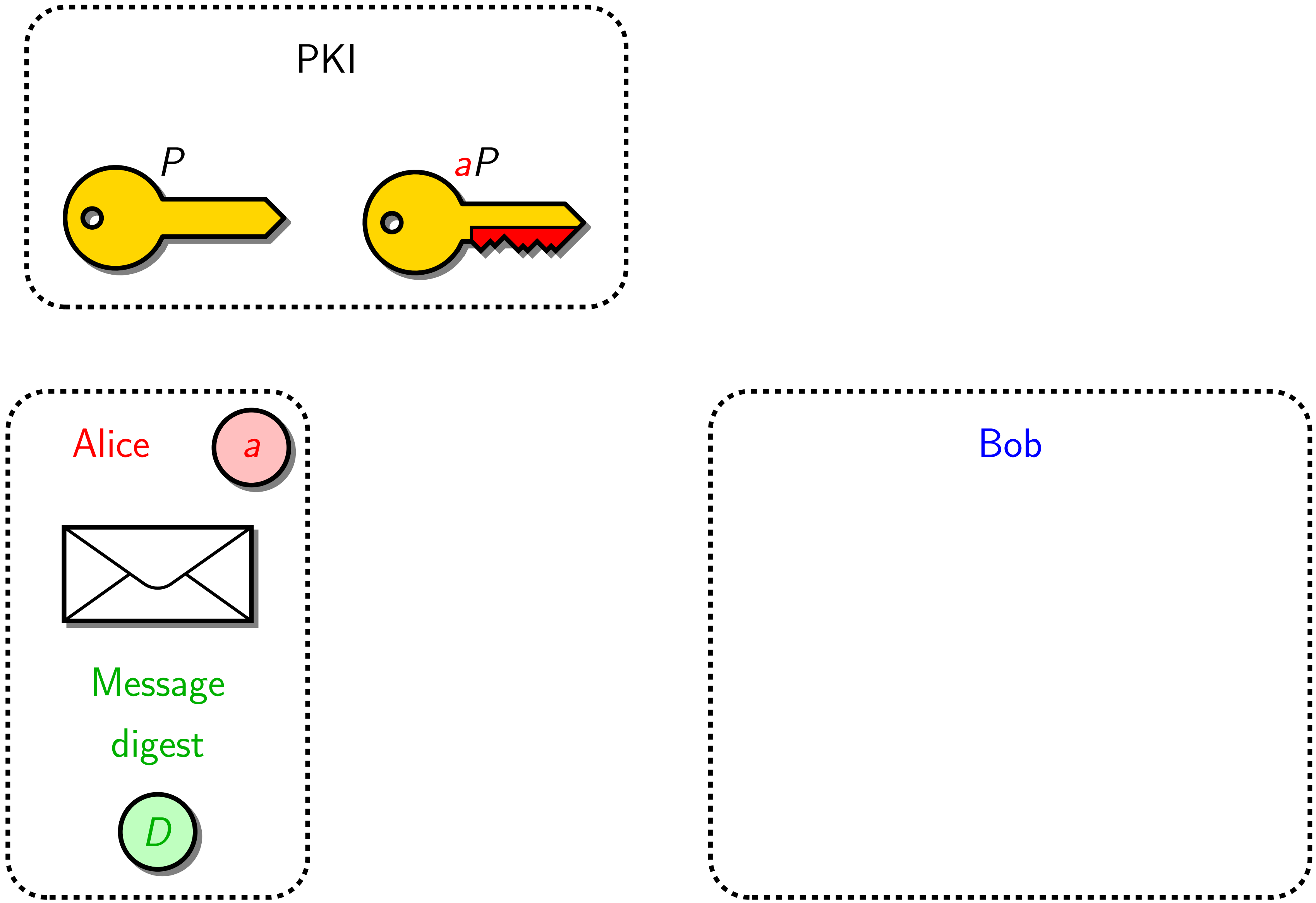

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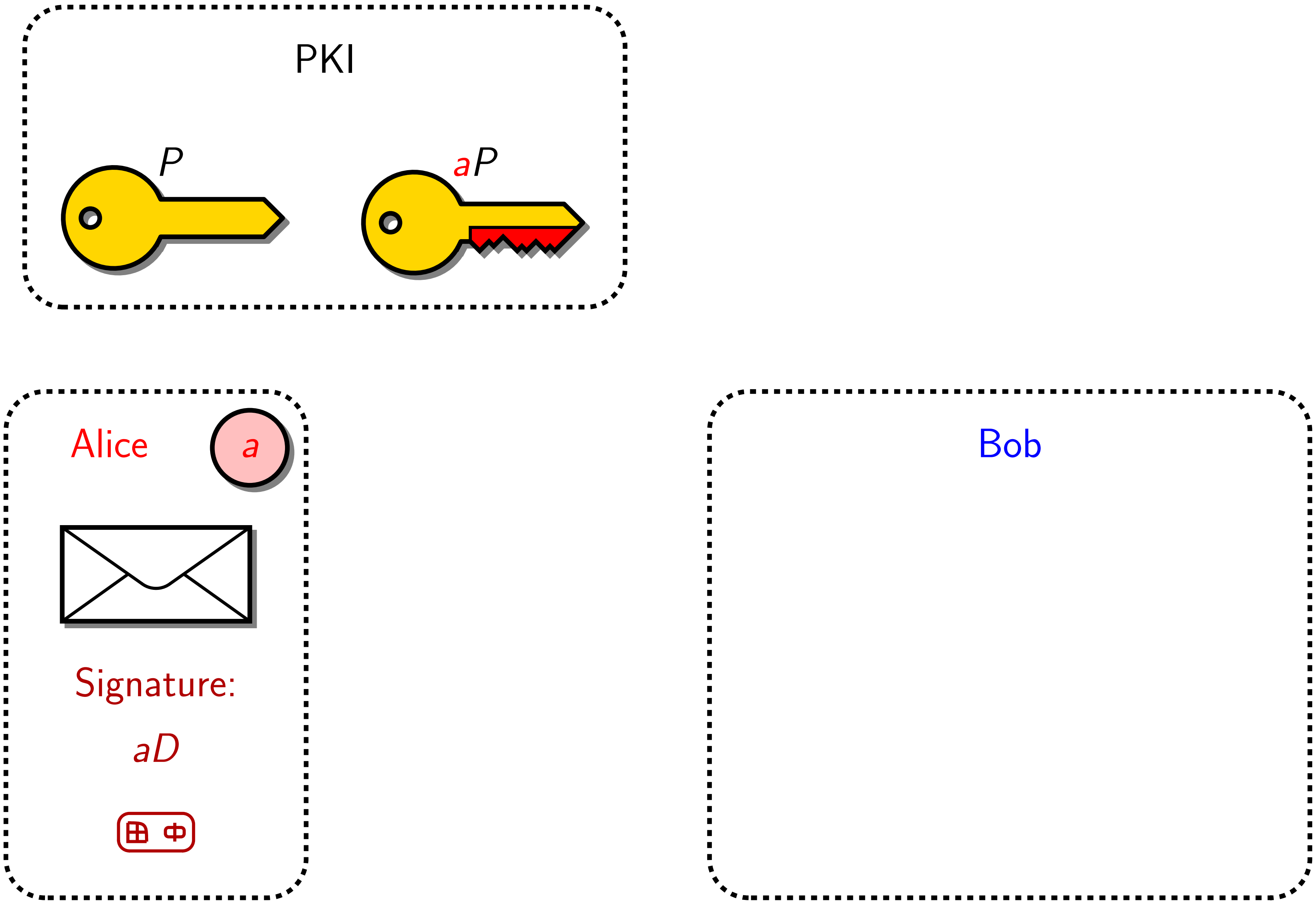

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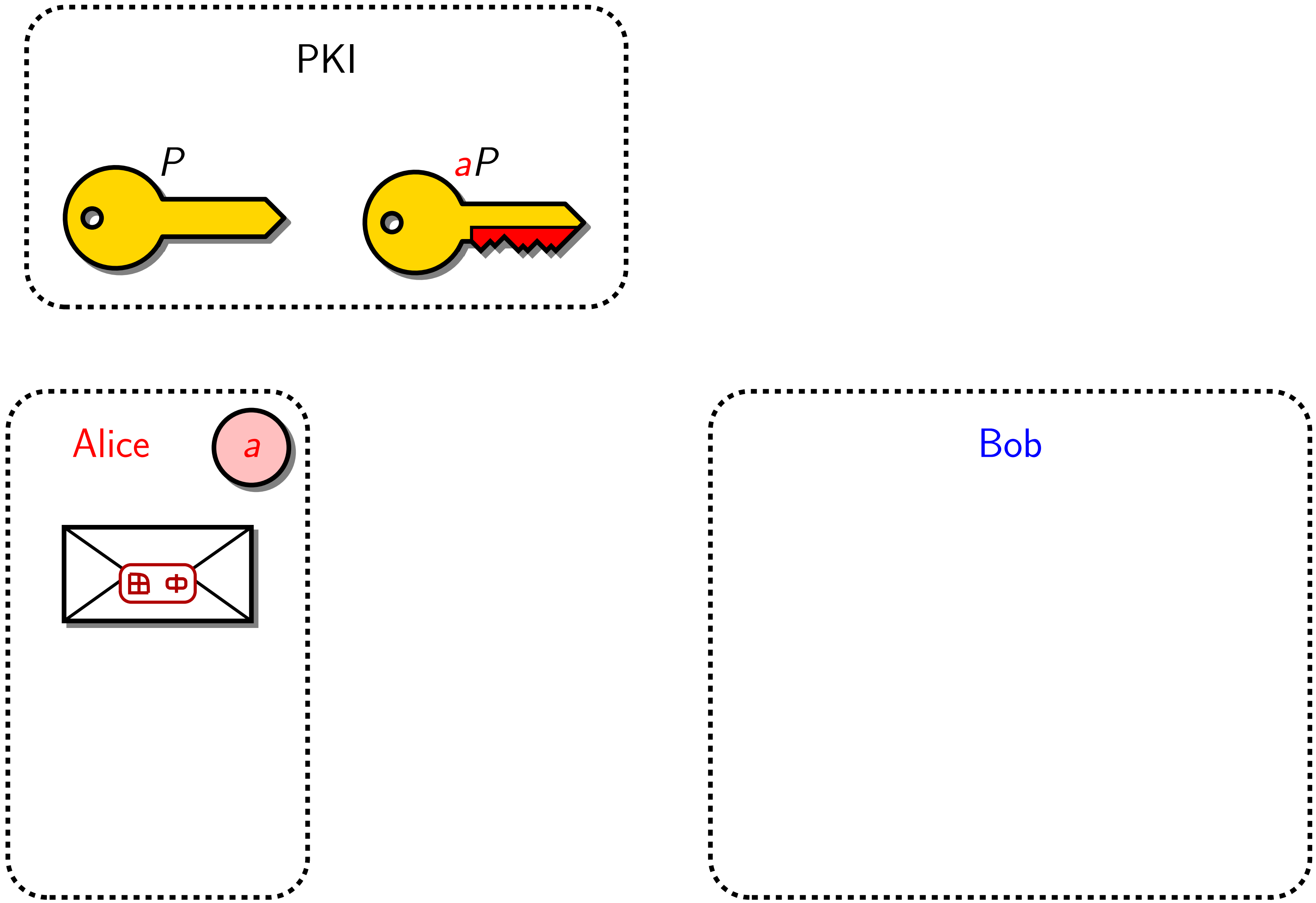

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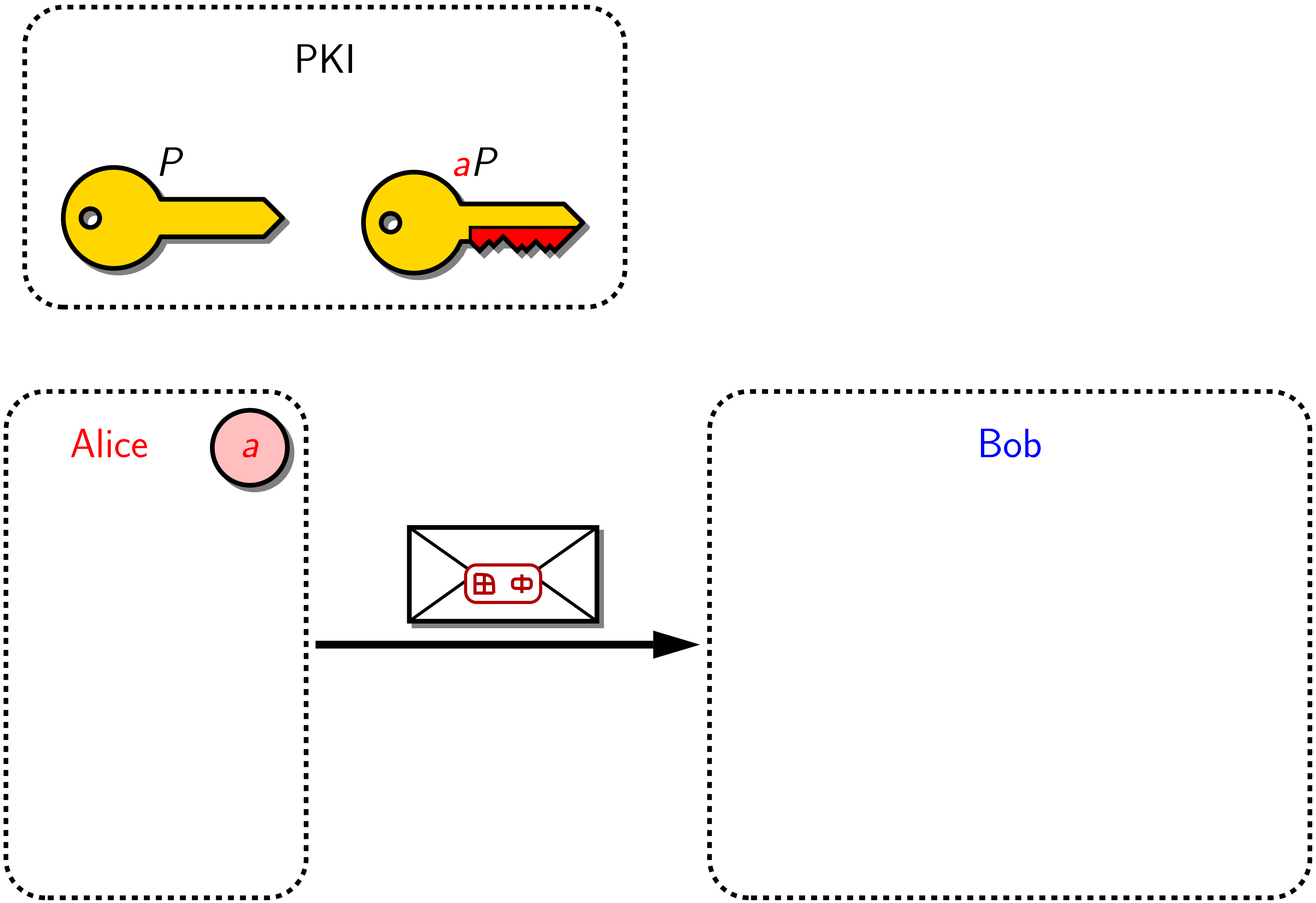

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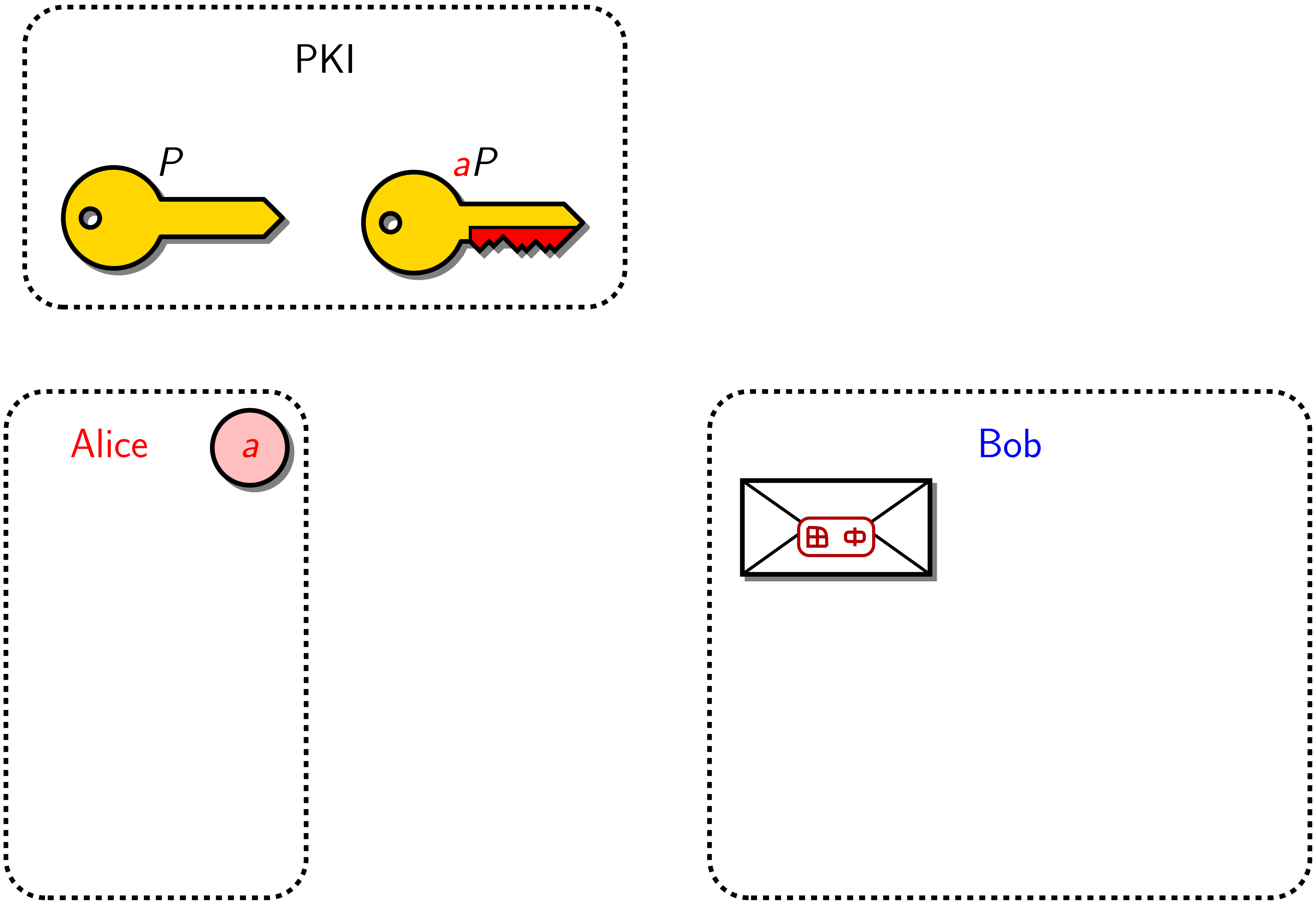

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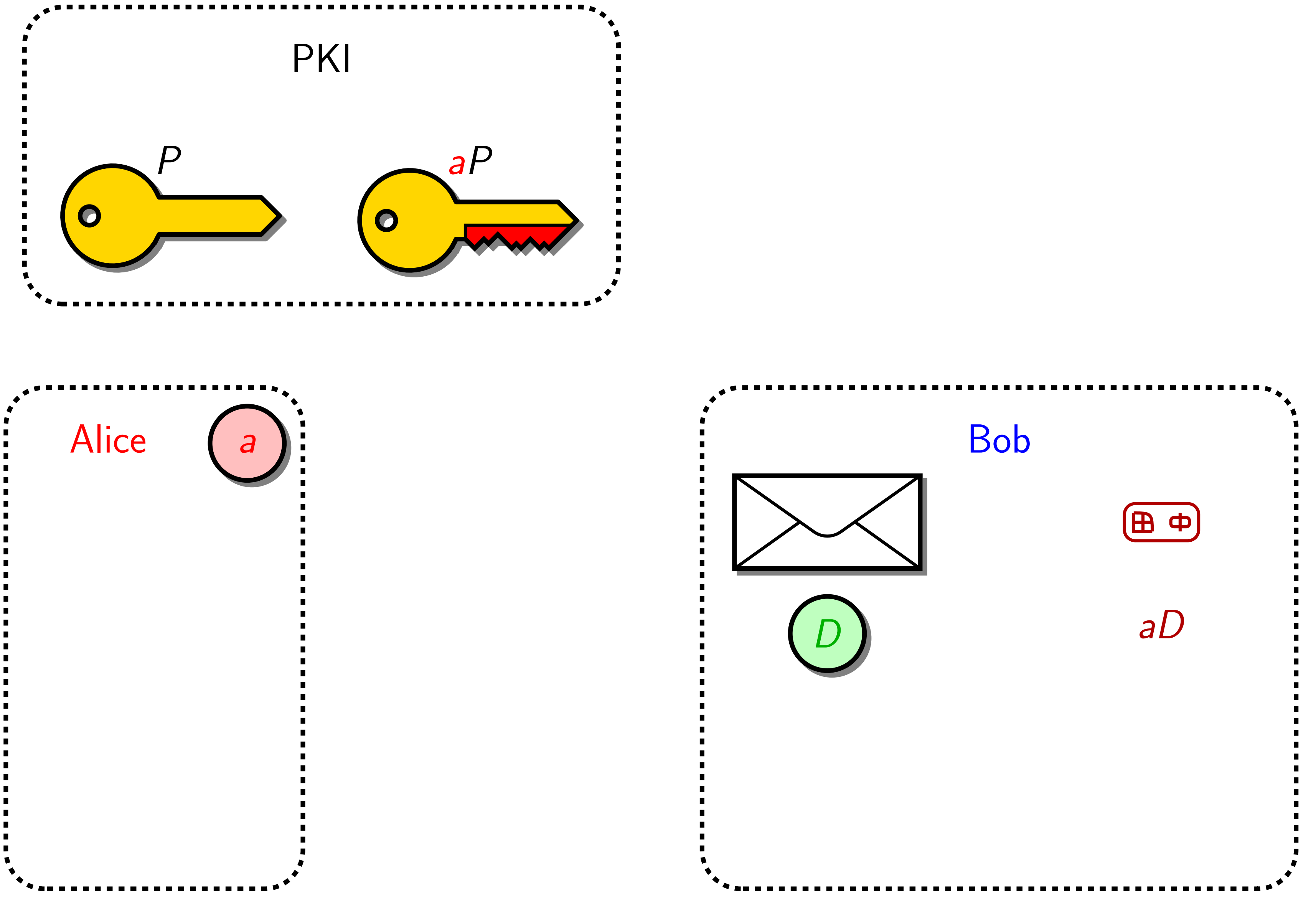

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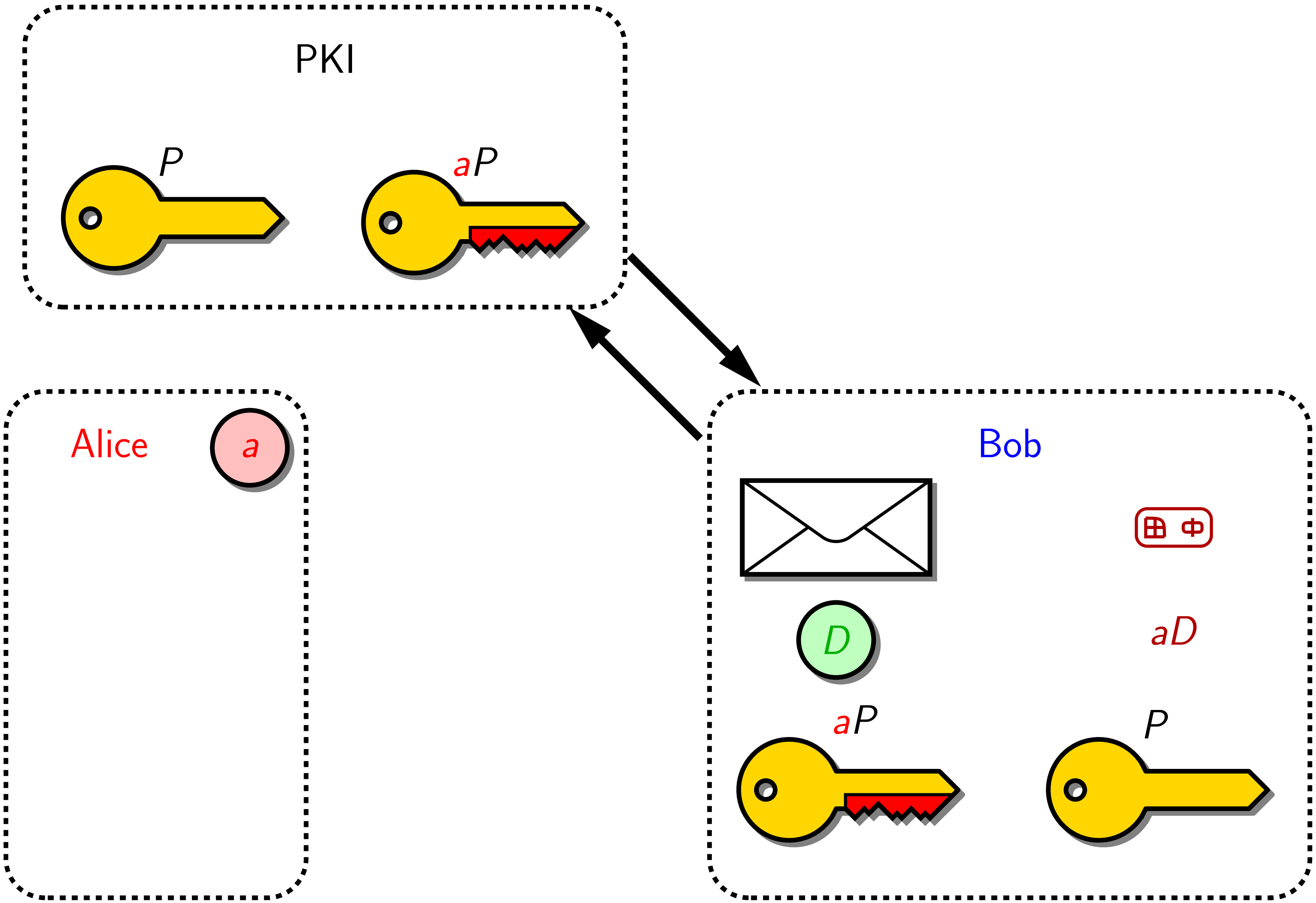

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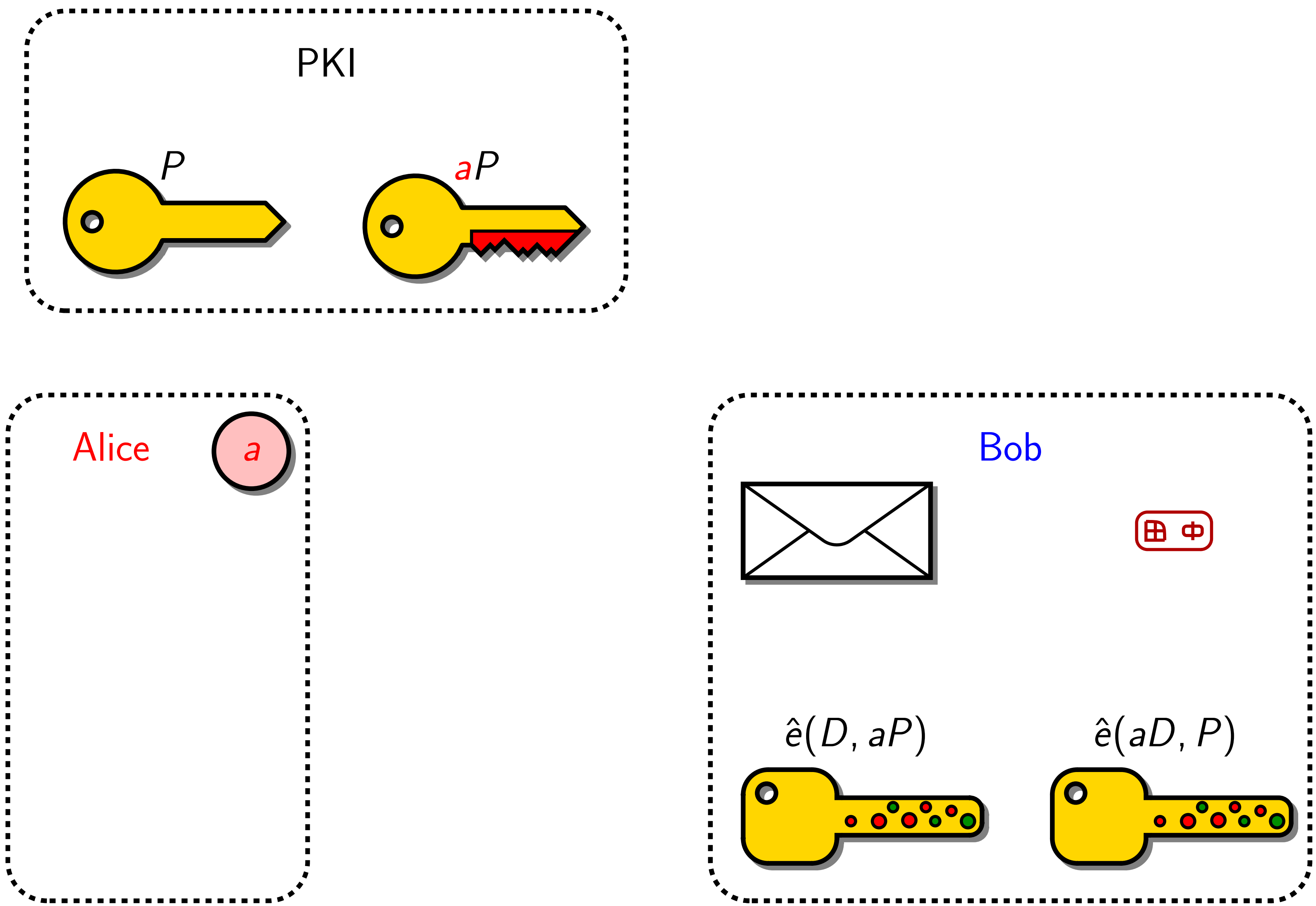

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  - $\mathbb{F}_q$, a finite field, with $q = 2^m$, 3^m or p
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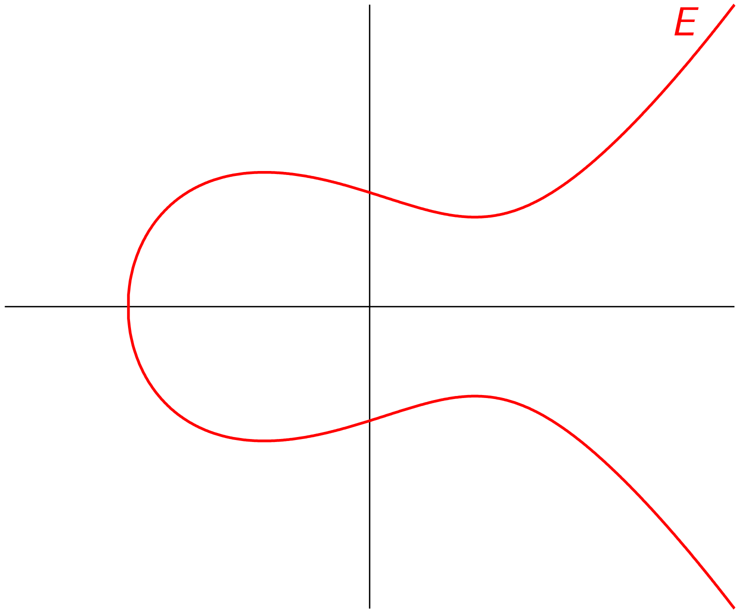
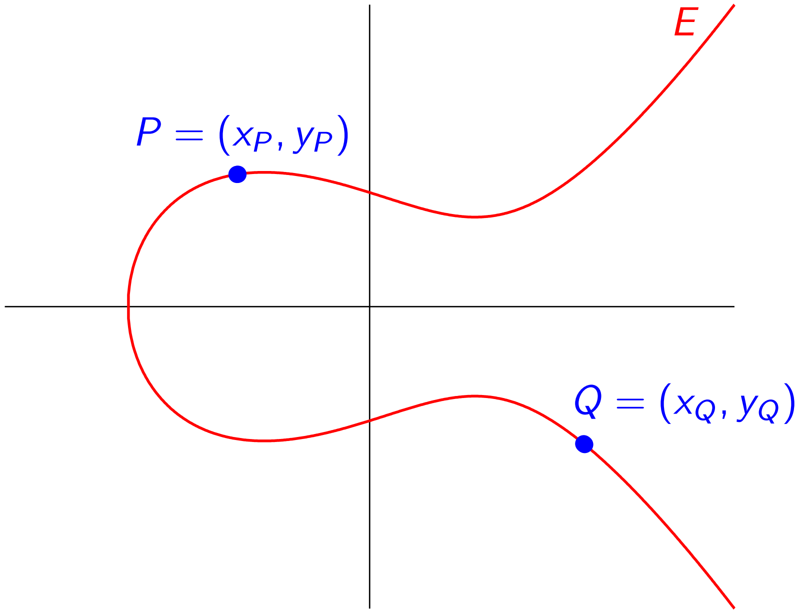
The Tate pairing



$\hat{e}$

The Tate pairing



$$\begin{array}{ccccc} \hat{e} & : & E(\mathbb{F}_q)[\ell] & \times & E(\mathbb{F}_q)[\ell] \\ & & (\quad P & , & Q \quad) \end{array}$$

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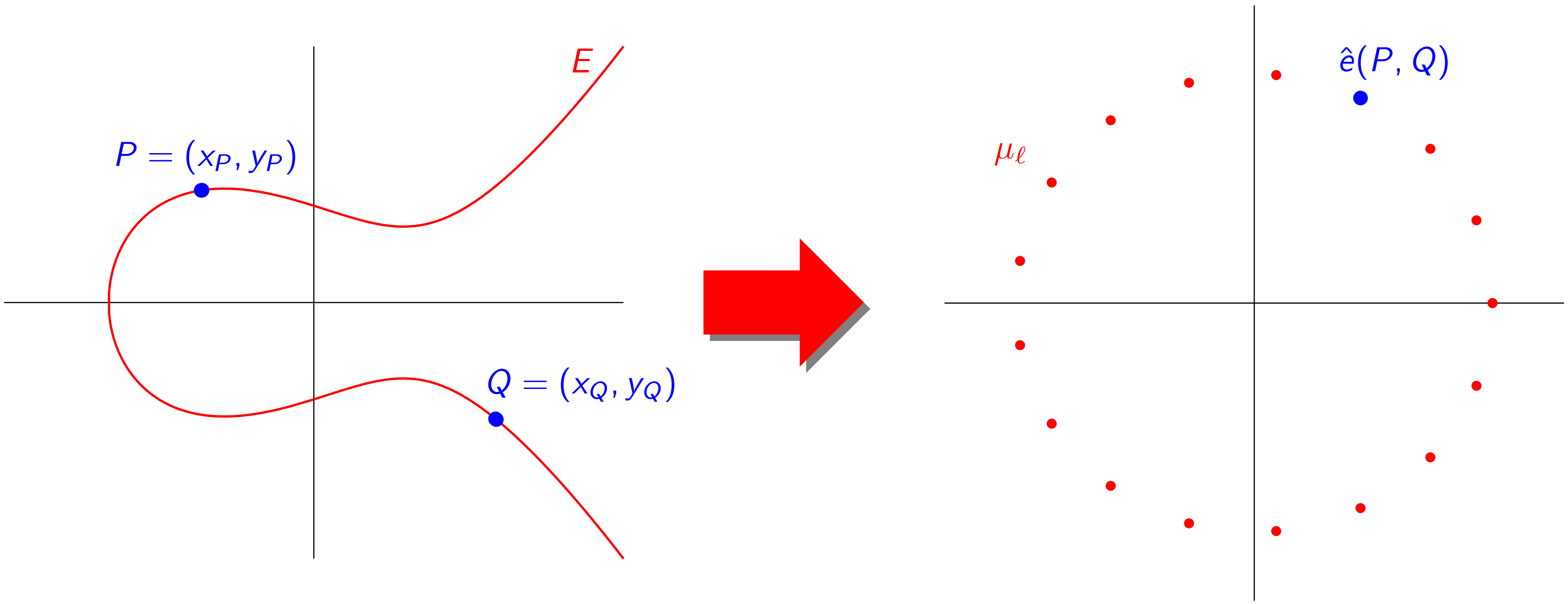

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\begin{array}{rccccc}
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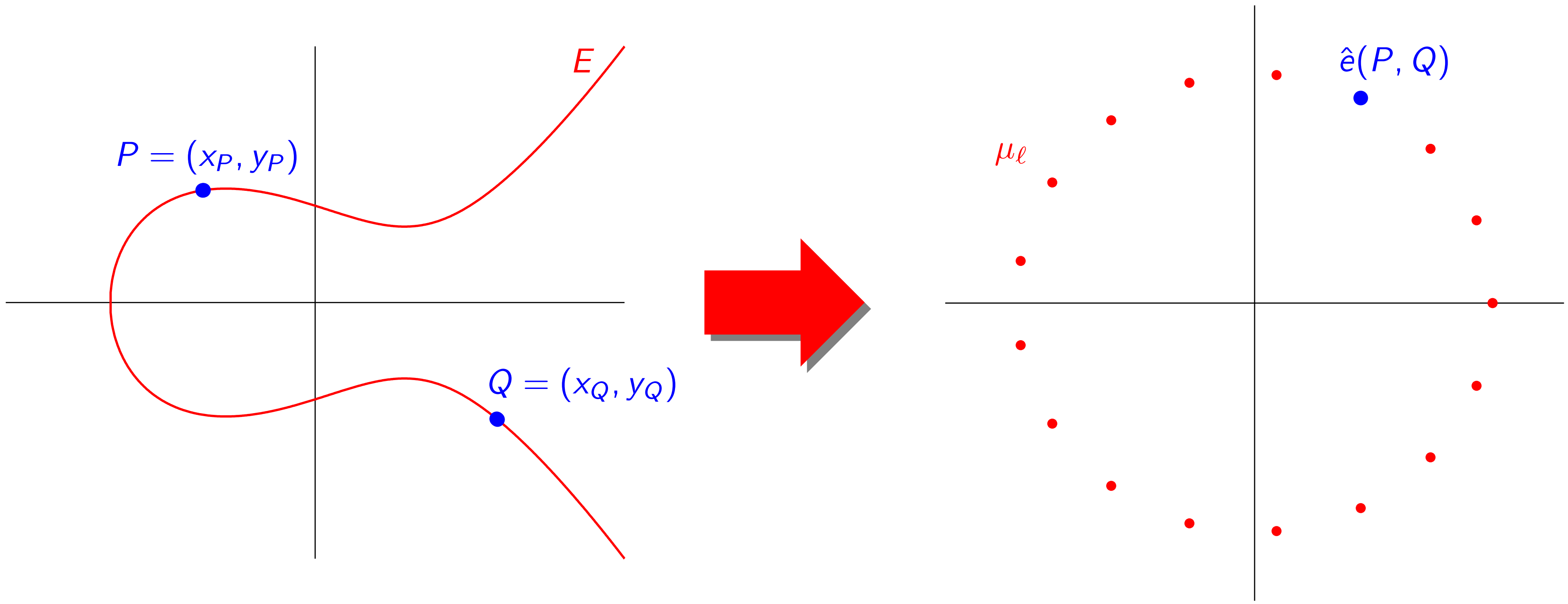

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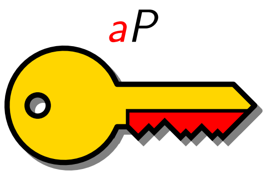
- Computation via Miller's iterative algorithm:
  - $m/2$ iterations over $\mathbb{F}_{2^m}$ and $\mathbb{F}_{3^m}$ (η_T pairing)
  - $\log_2 p$ iterations over $\mathbb{F}_p$

Security considerations



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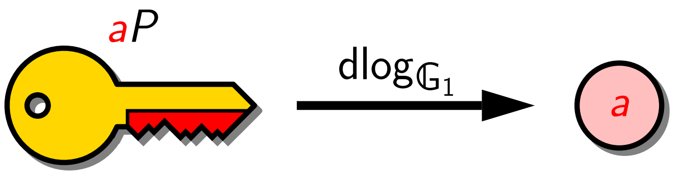

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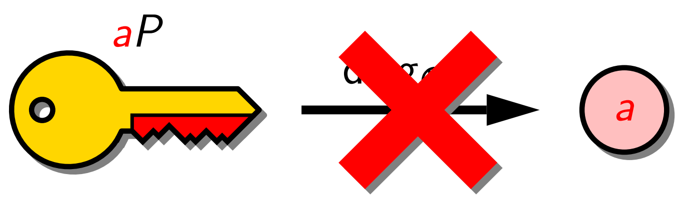

- Discrete logarithm problem should be hard in $\mathbb{G}_1$

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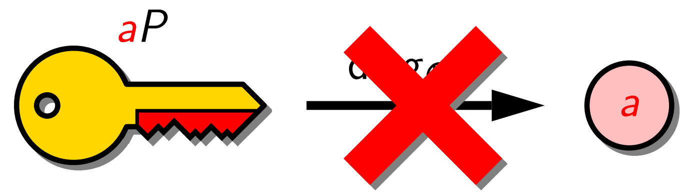

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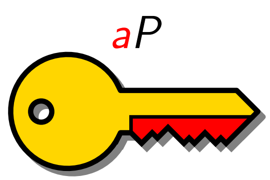

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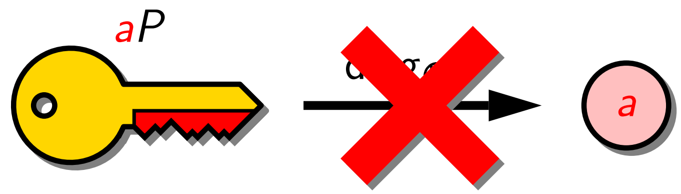

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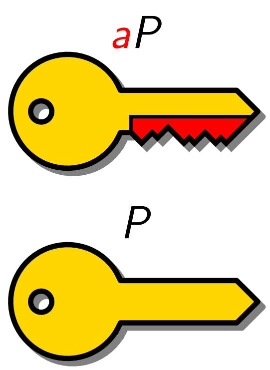

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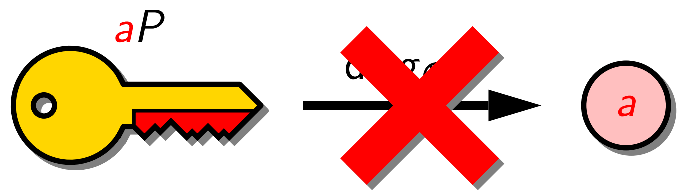

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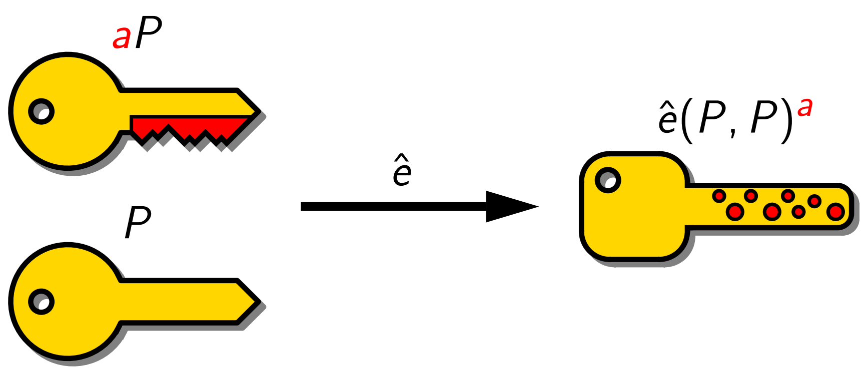

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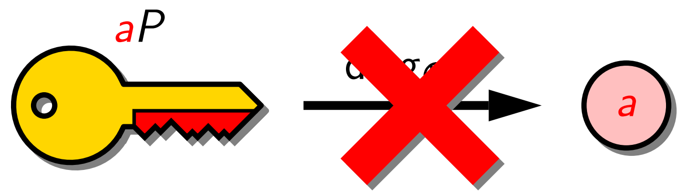

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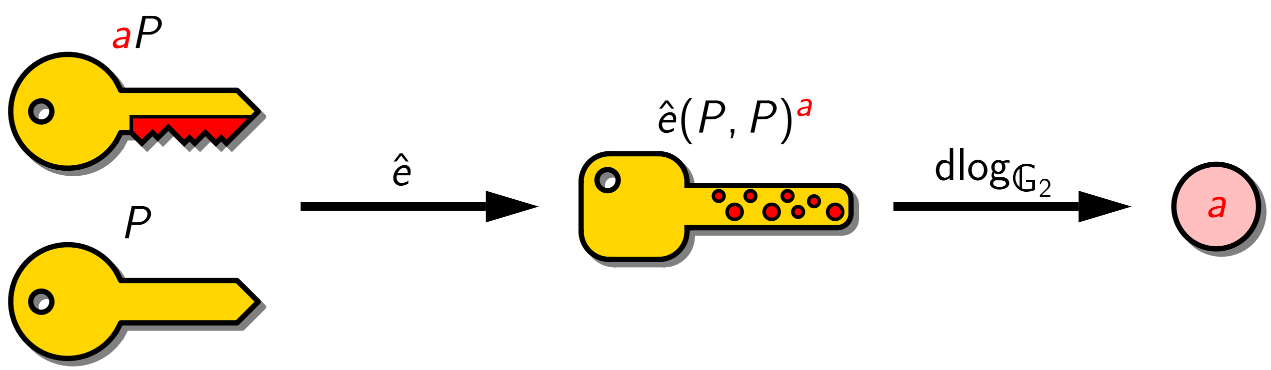

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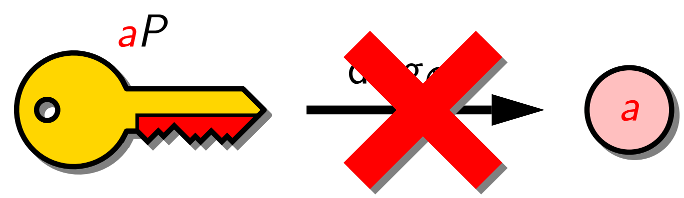

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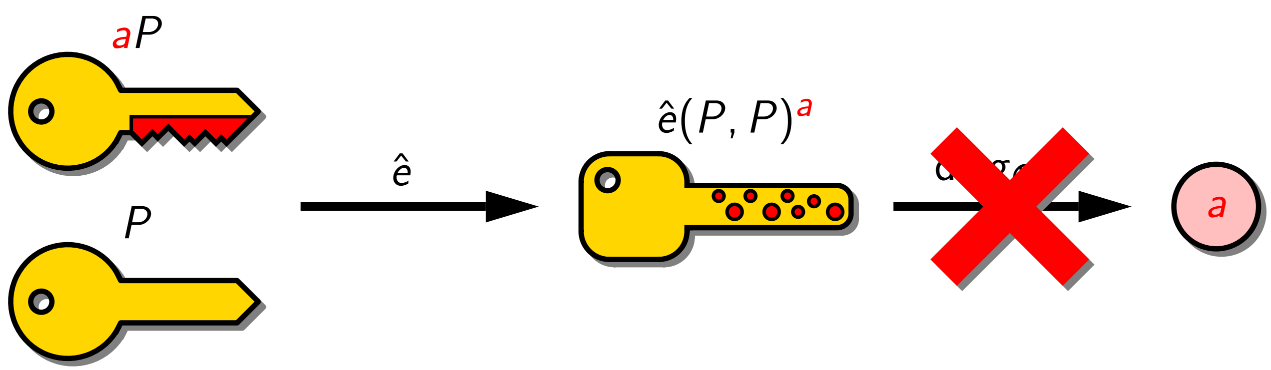

- Discrete logarithm problem should be hard in $\mathbb{G}_2$

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$$\sqrt{\ell} \approx \sqrt{q}$$

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- The discrete logarithm problem is usually easier in $\mathbb{G}_2$ than in $\mathbb{G}_1$
  - current security: $\sim 2^{80}$, equivalent to 80-bit symmetric encryption or RSA-1024
  - recommended security: $\sim 2^{128}$ (AES-128, RSA-3072)

Security considerations

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$\times$	$7\lfloor \frac{m}{2} \rfloor + 29$	1121	$25\lfloor \frac{m}{4} \rfloor + 93$	868
a^p	$6m + 9$	1887	$17\lfloor \frac{m}{2} \rfloor + 8$	1079
a^{-1}	1	1	1	1

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- Software not well suited to small characteristic: need for hardware acceleration

Outline of the talk

- Pairing-based cryptography
- Pairings over elliptic curves
- Finite-field arithmetic
- Implementation results
- Concluding thoughts

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Arithmetic over $\mathbb{F}_{3^m}$

- $f \in \mathbb{F}_3[x]$: degree-m irreducible polynomial over $\mathbb{F}_3$

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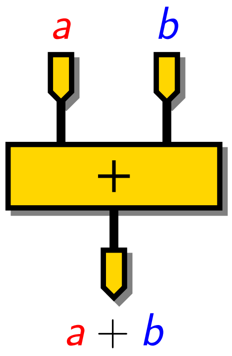
- $\mathbb{F}_{3^m} \cong \mathbb{F}_3[x]/(f)$
- $a \in \mathbb{F}_{3^m}$:

$$a = a_{m-1}x^{m-1} + \cdots + a_1 x + a_0$$

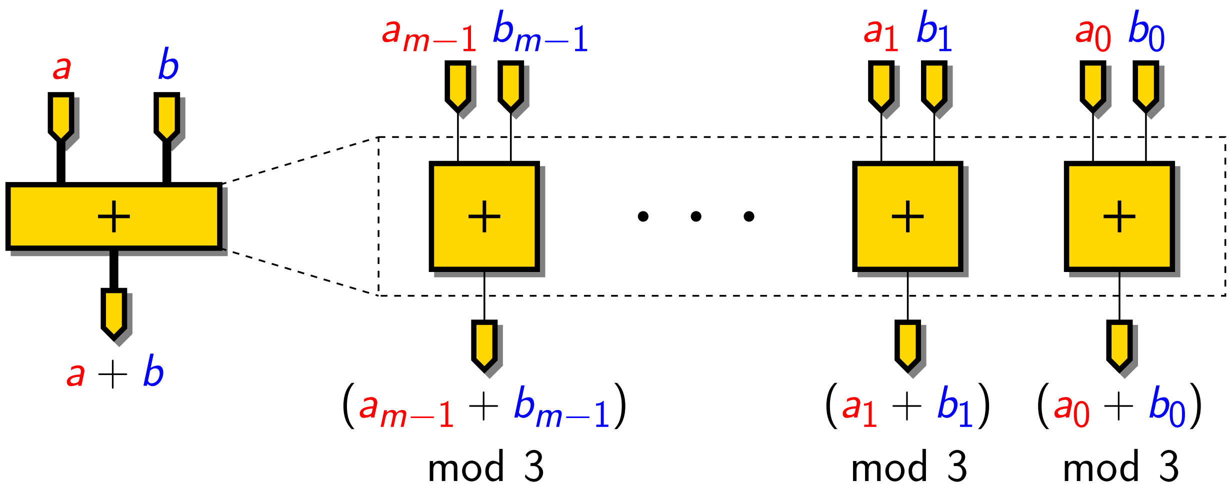
- Each element of $\mathbb{F}_3$ stored using two bits

Addition over $\mathbb{F}_{3^m}$



- $r = a + b = (a_{m-1} + b_{m-1})x^{m-1} + \cdots + (a_1 + b_1)x + (a_0 + b_0)$

Addition over $\mathbb{F}_{3^m}$



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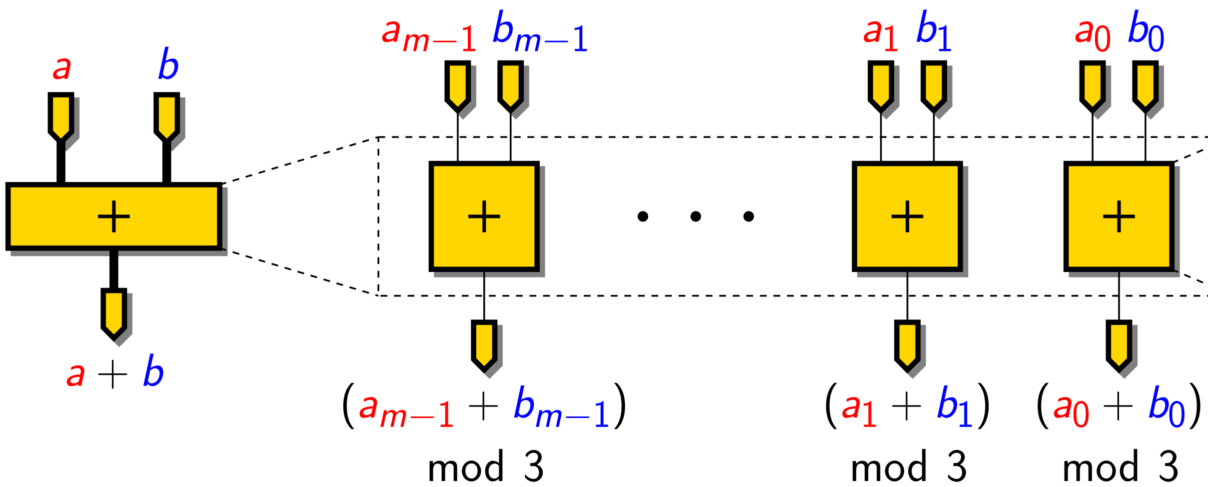

+	0	1	2
0	0	1	2
1	1	2	0
2	2	0	1

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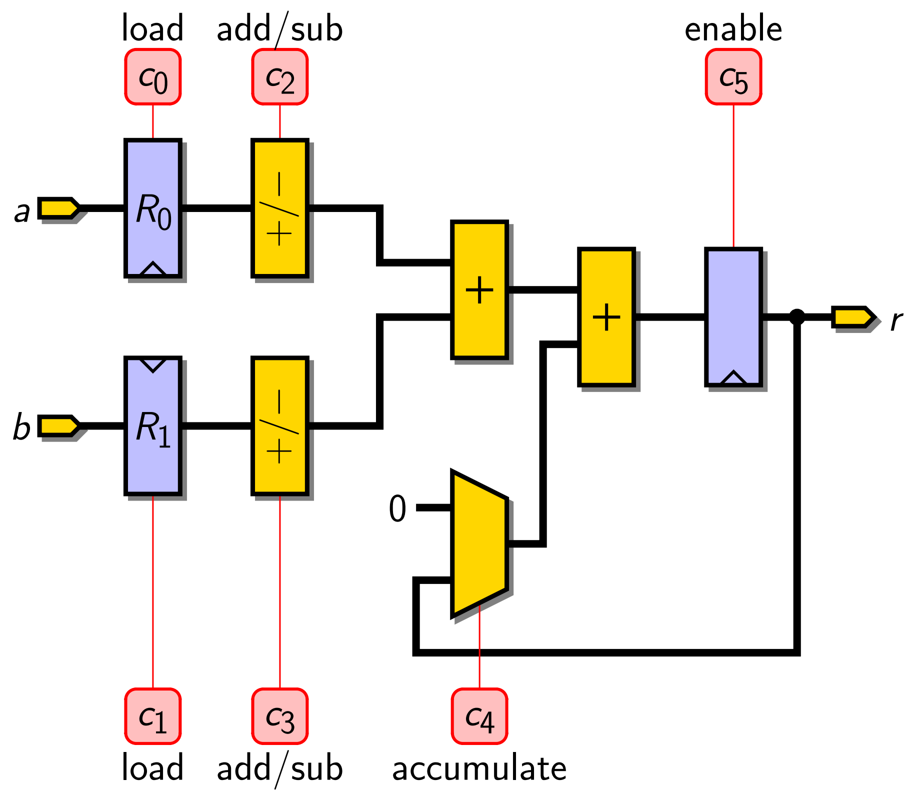
  - coefficient-wise additions over $\mathbb{F}_3$: $r_i = (a_i + b_i) \bmod 3$
  - addition over $\mathbb{F}_3$: small look-up tables

Addition, subtraction and accumulation over $\mathbb{F}_{3^m}$



- sign selection: multiplication by 1 or 2

$$-a \equiv 2a \pmod 3$$

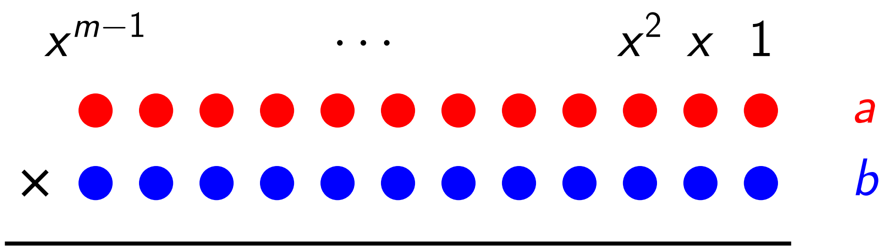
- feedback loop for accumulation

Multiplication over $\mathbb{F}_{3^m}$

- Parallel-serial multiplication
  - multiplicand loaded in a parallel register
  - multiplier loaded in a shift register
- Most significant coefficients first (Horner scheme)
- D coefficients processed at each clock cycle: $\left\lceil \frac{m}{D} \right\rceil$ cycles per multiplication

Multiplication over $\mathbb{F}_{3^m}$

- Example for $D = 3$ (3 coefficients per iteration):



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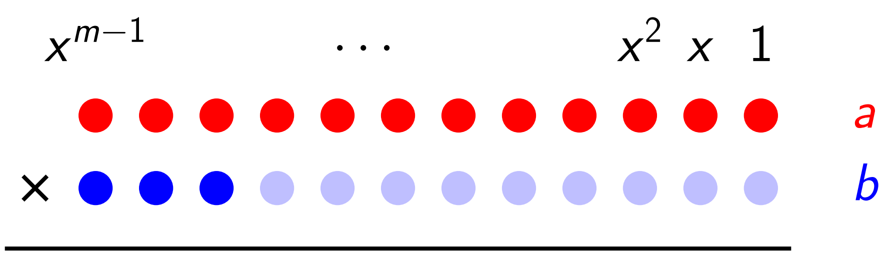

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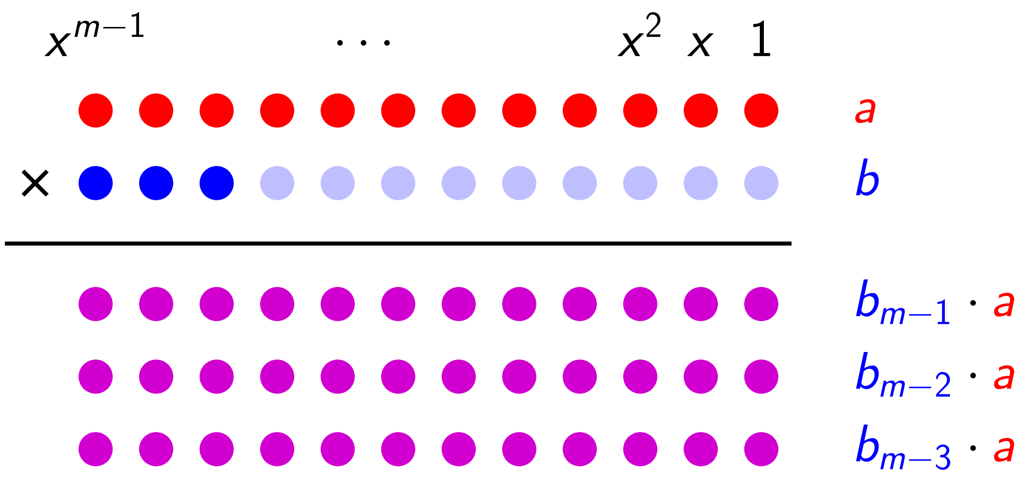

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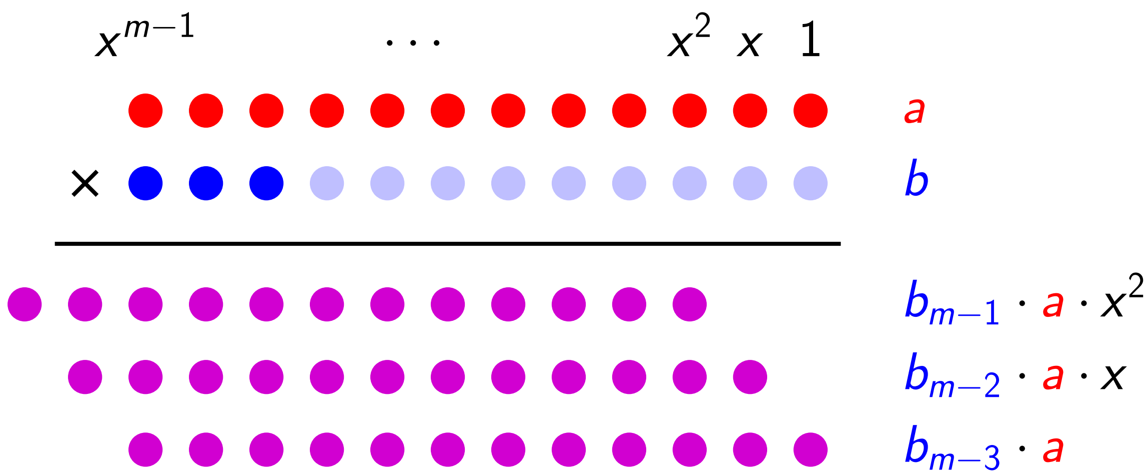

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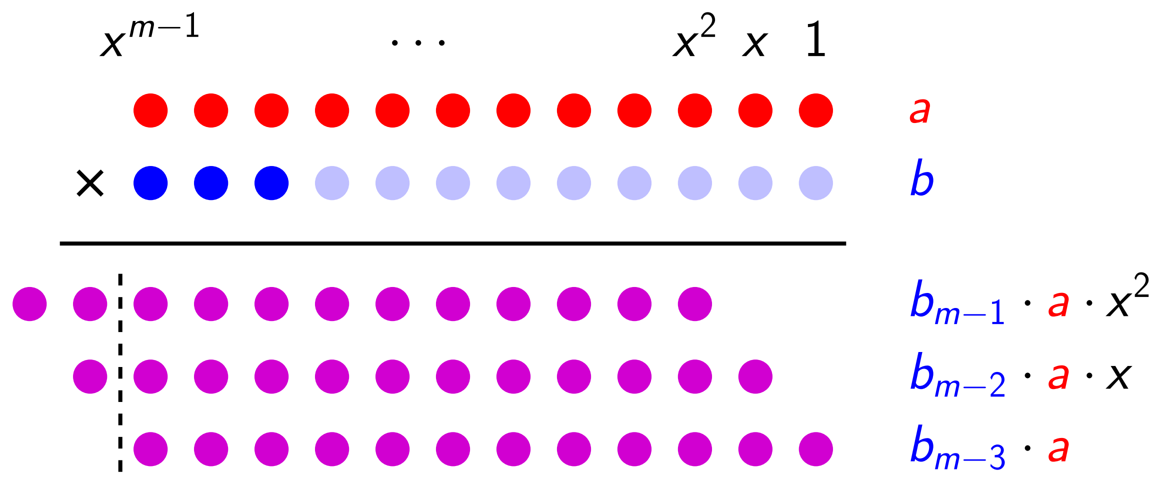

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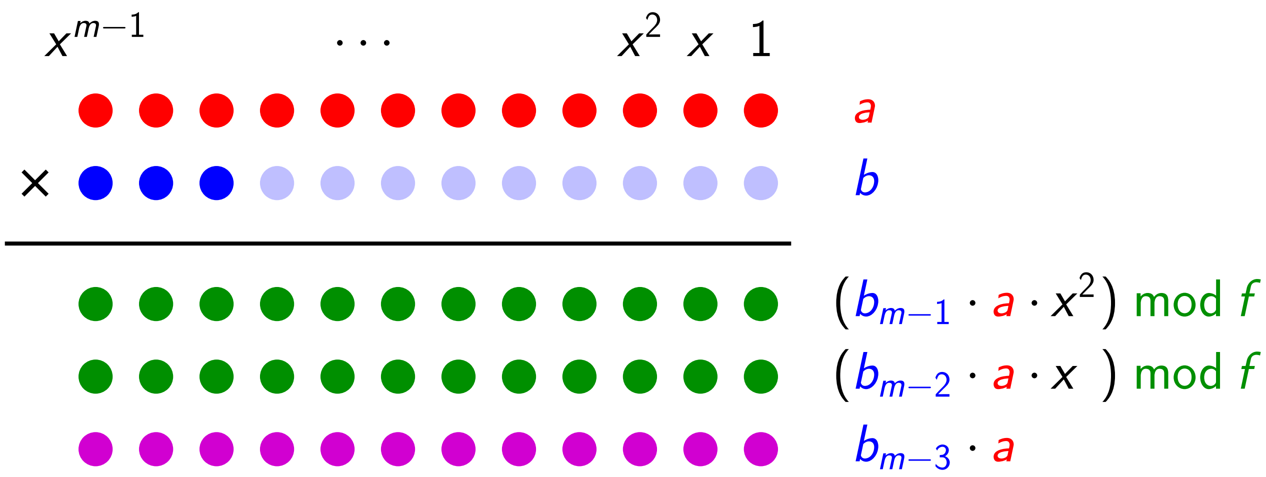

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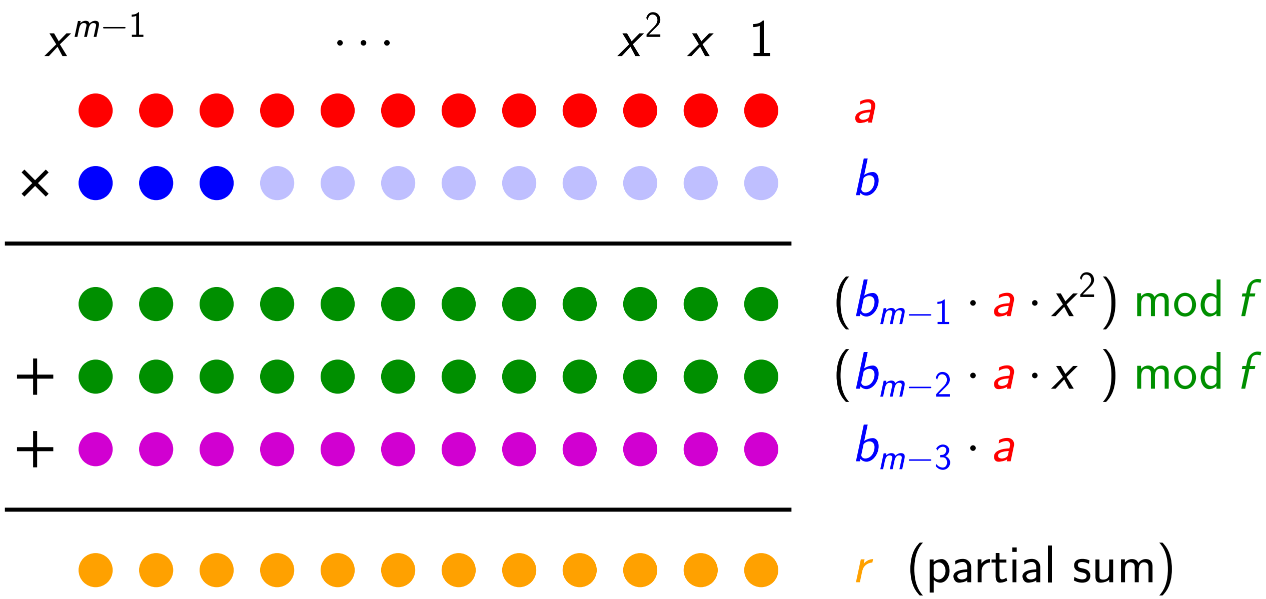

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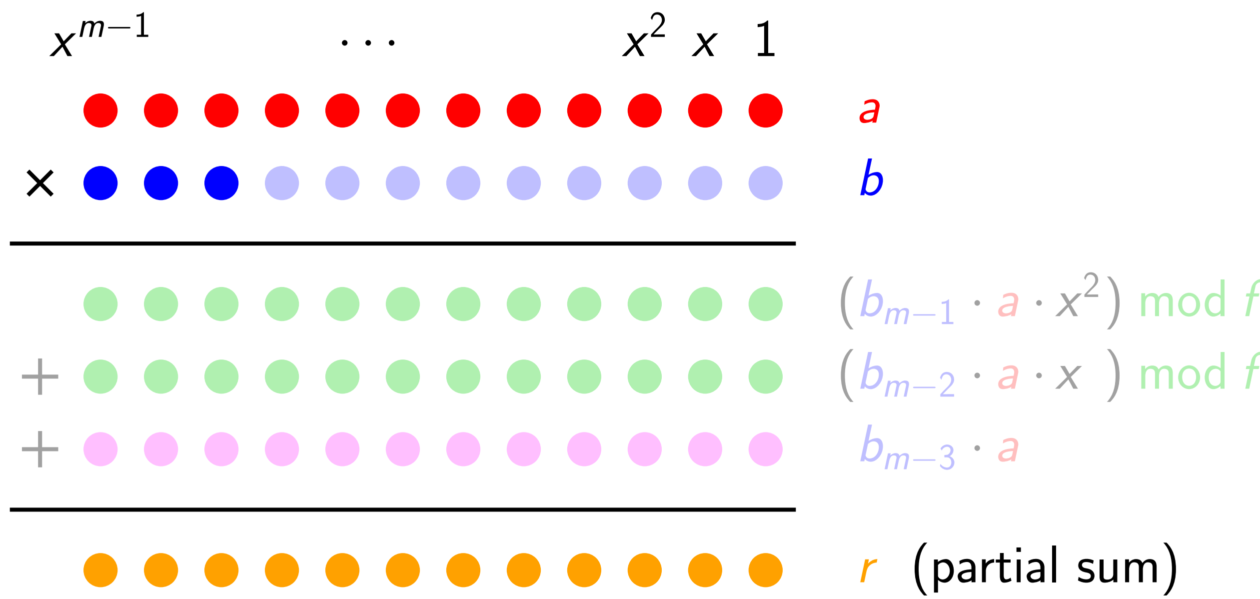

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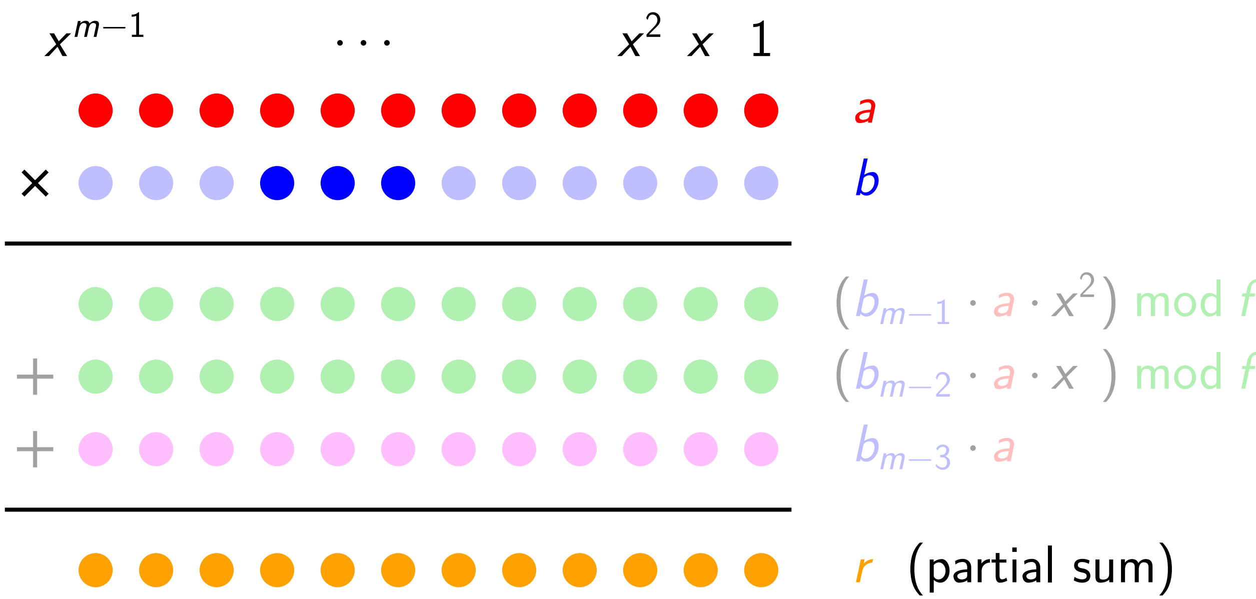

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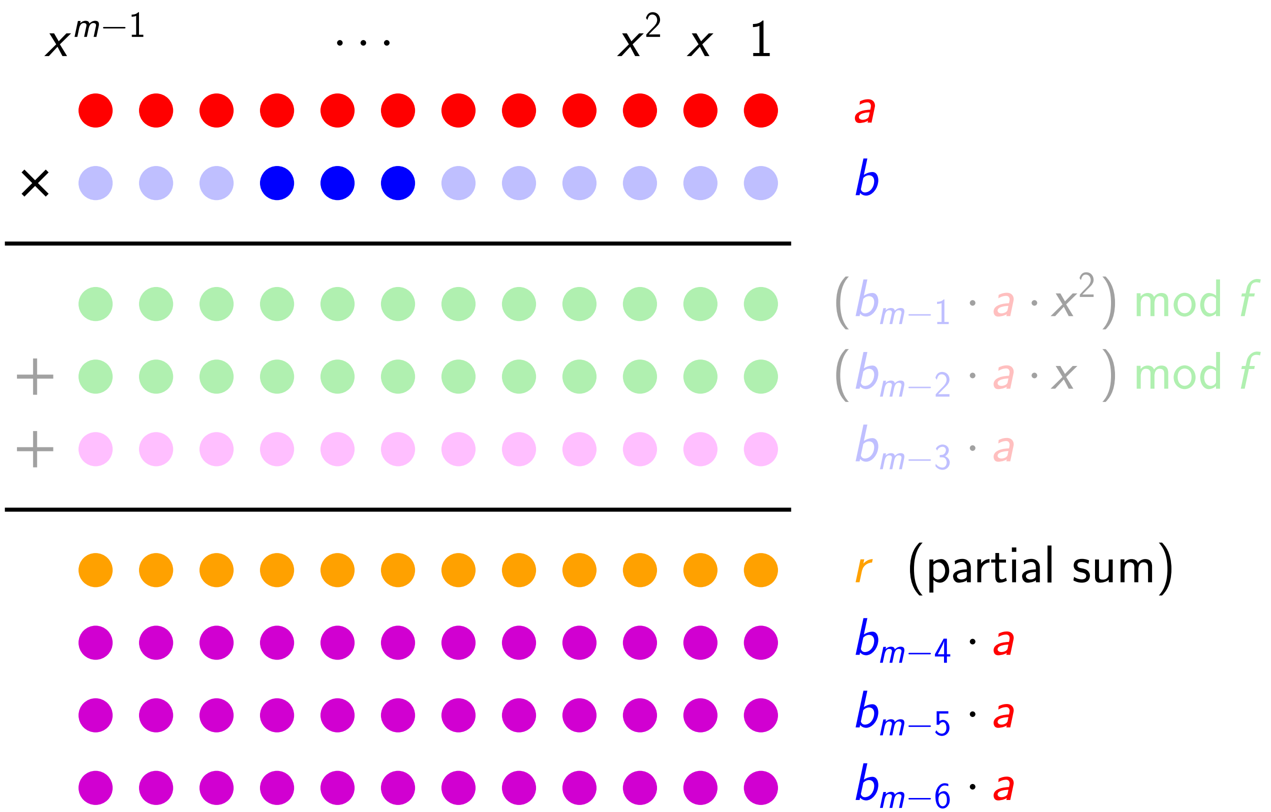

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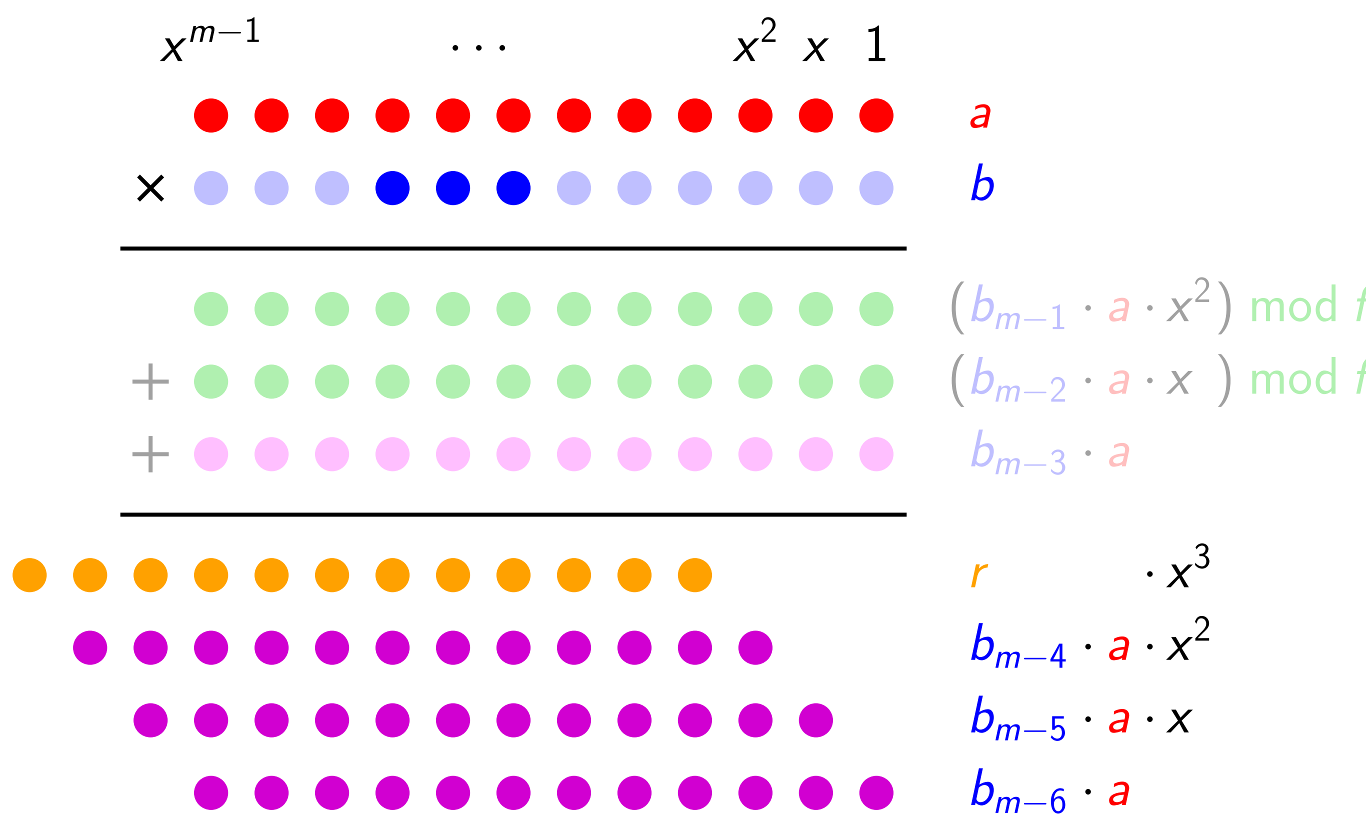
- Example for $D = 3$ (3 coefficients per iteration):



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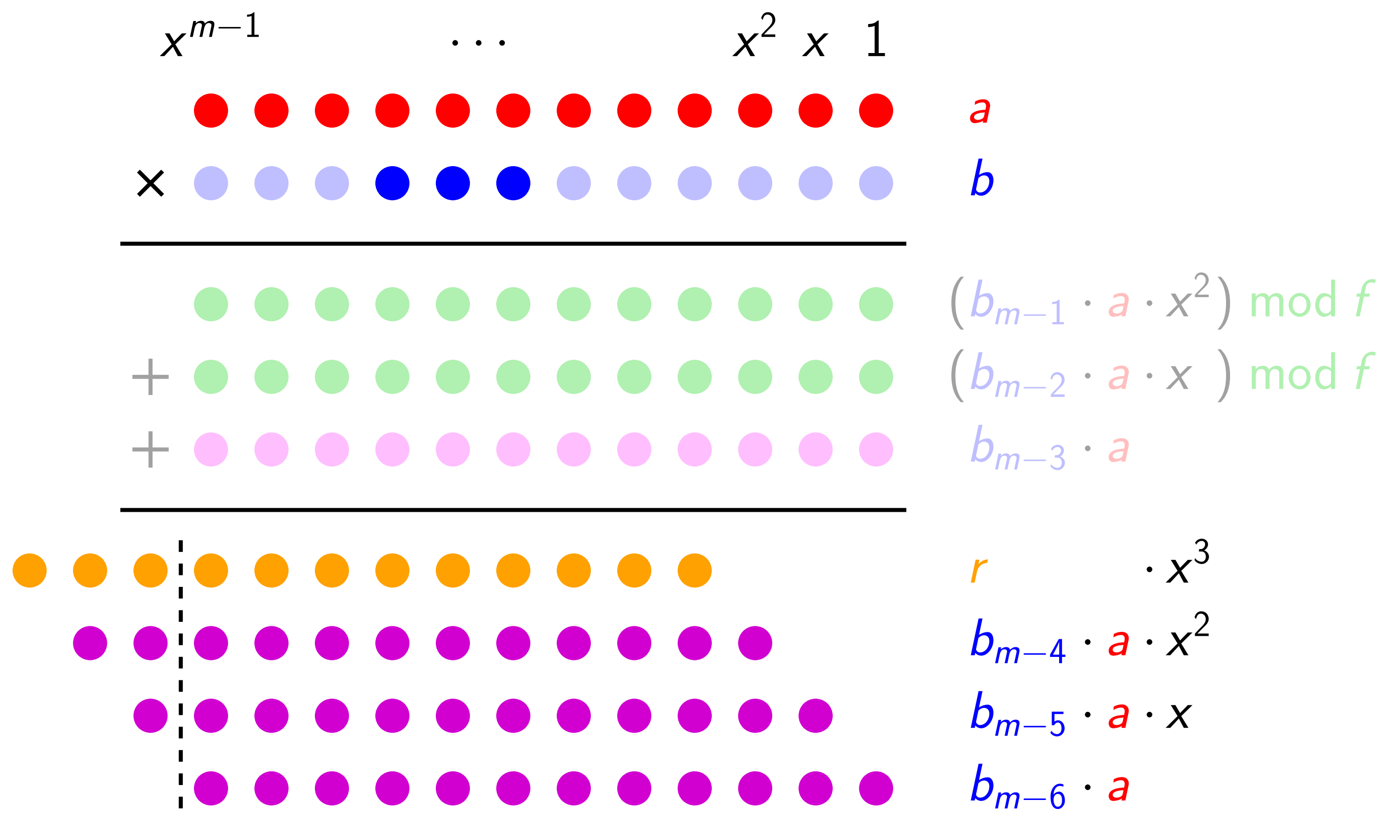

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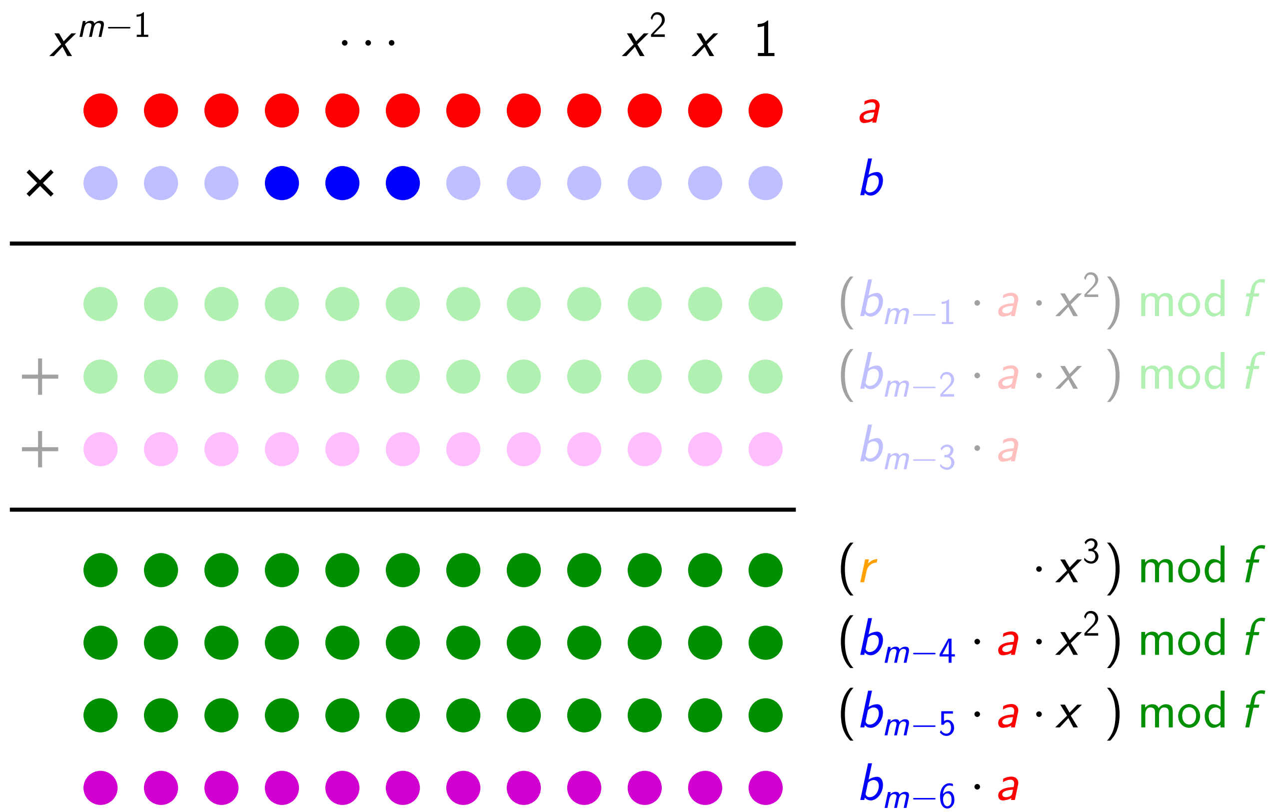

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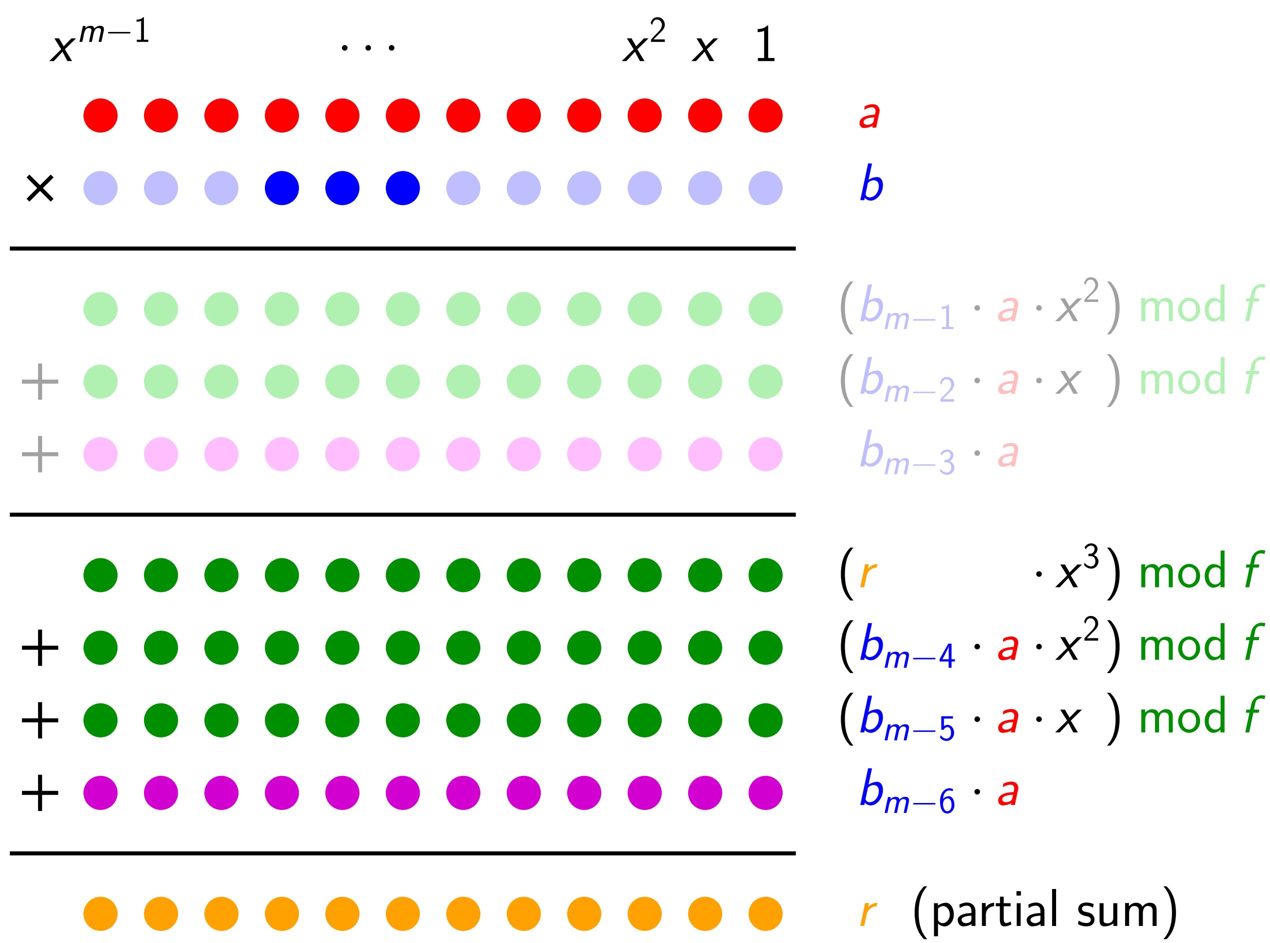

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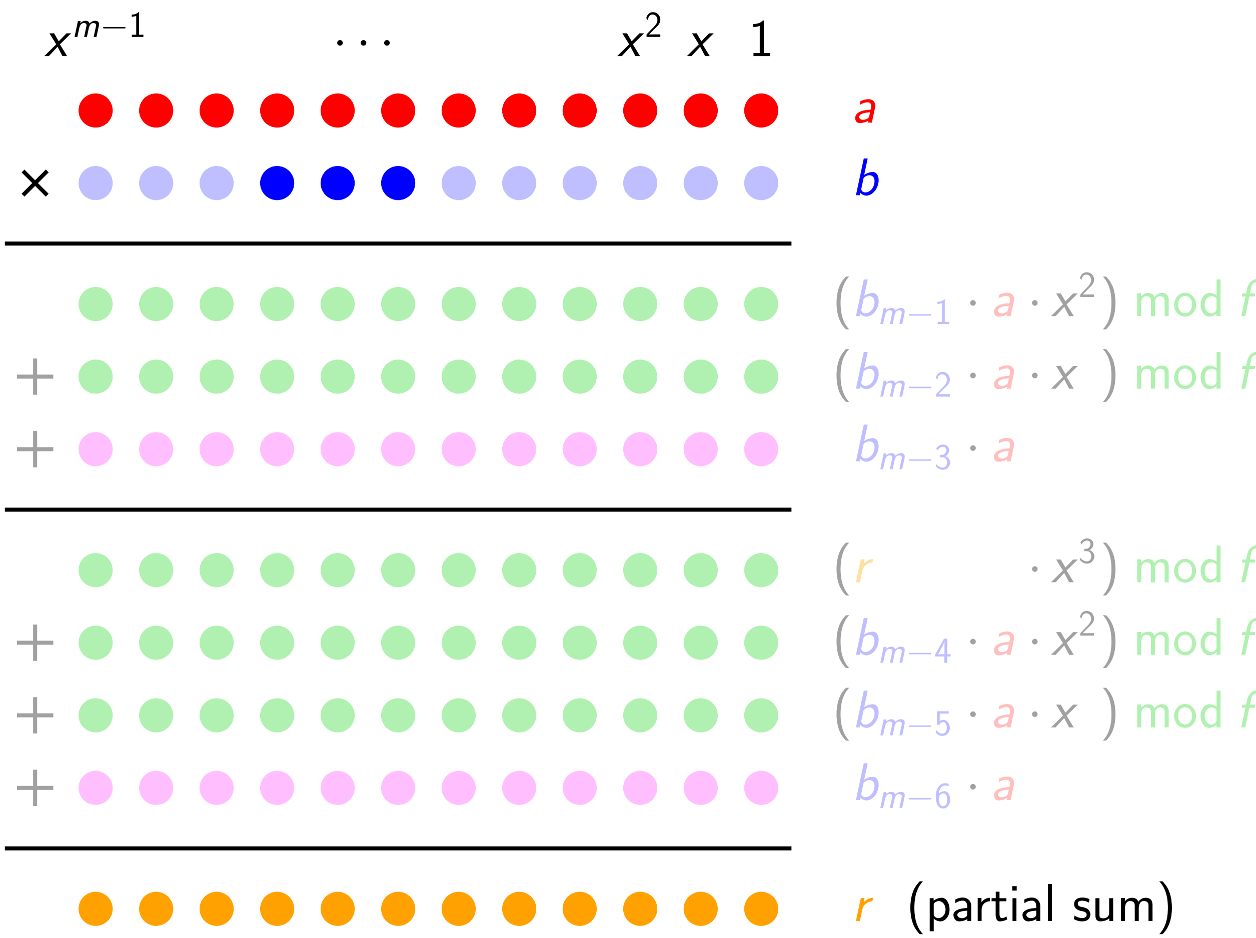

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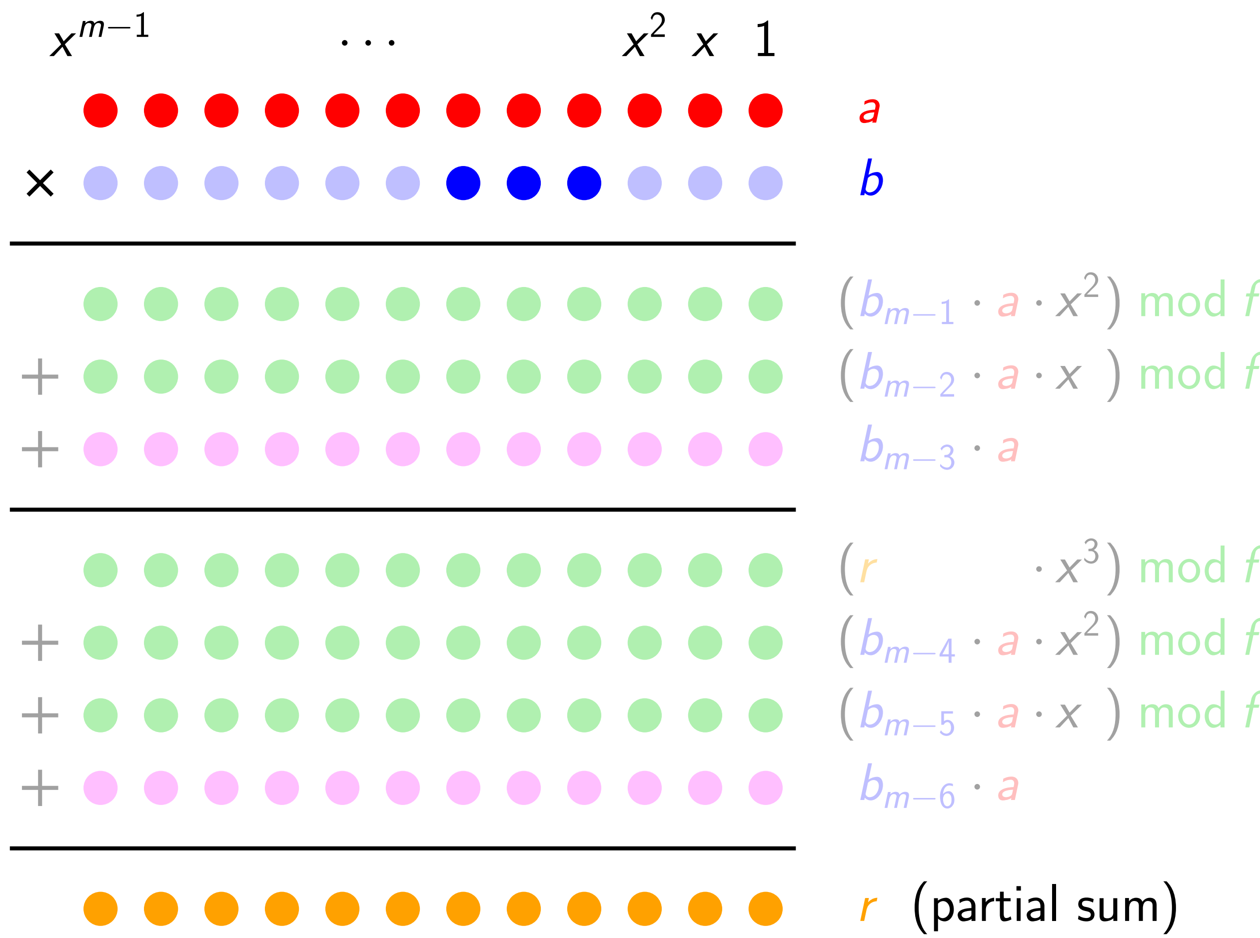

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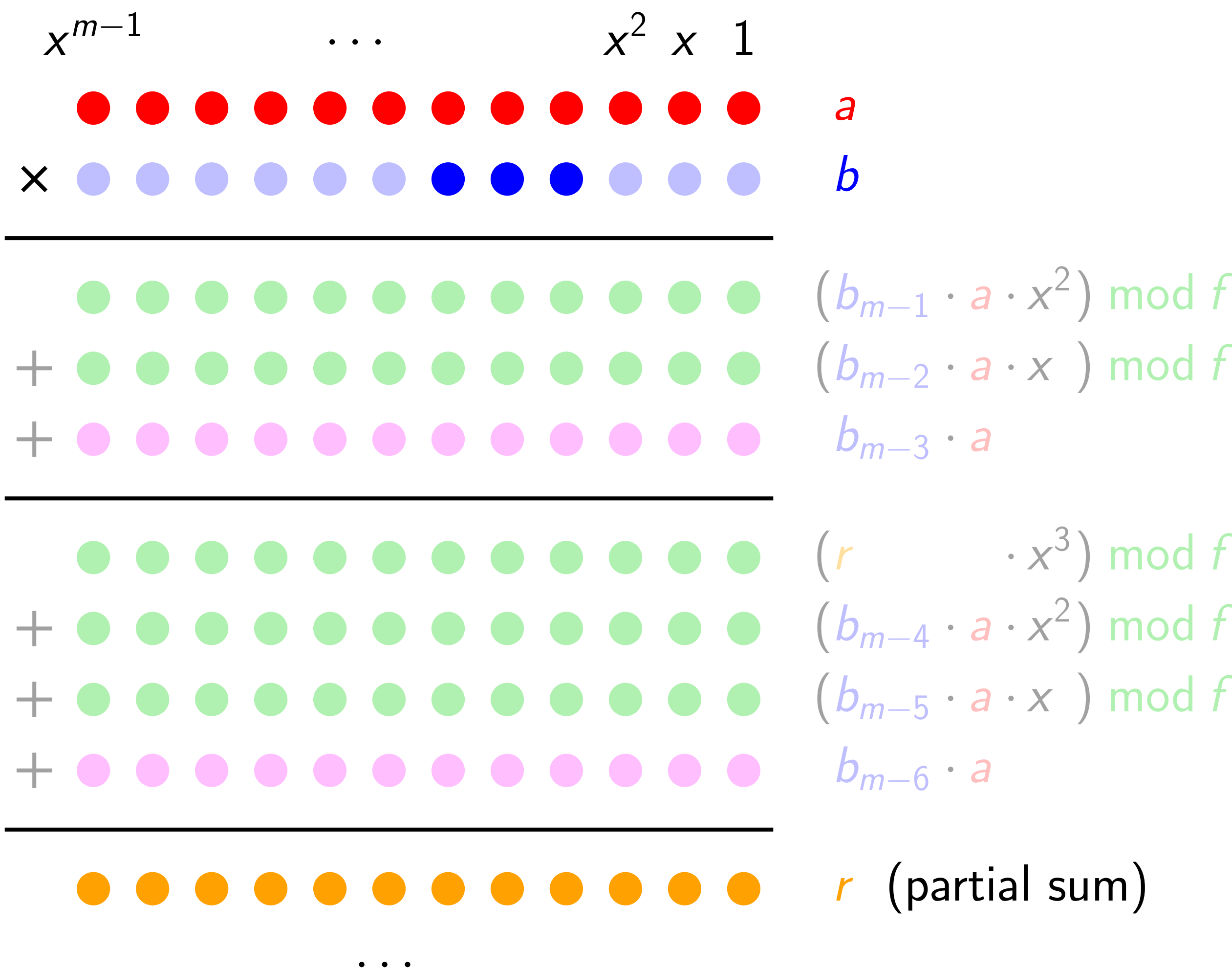

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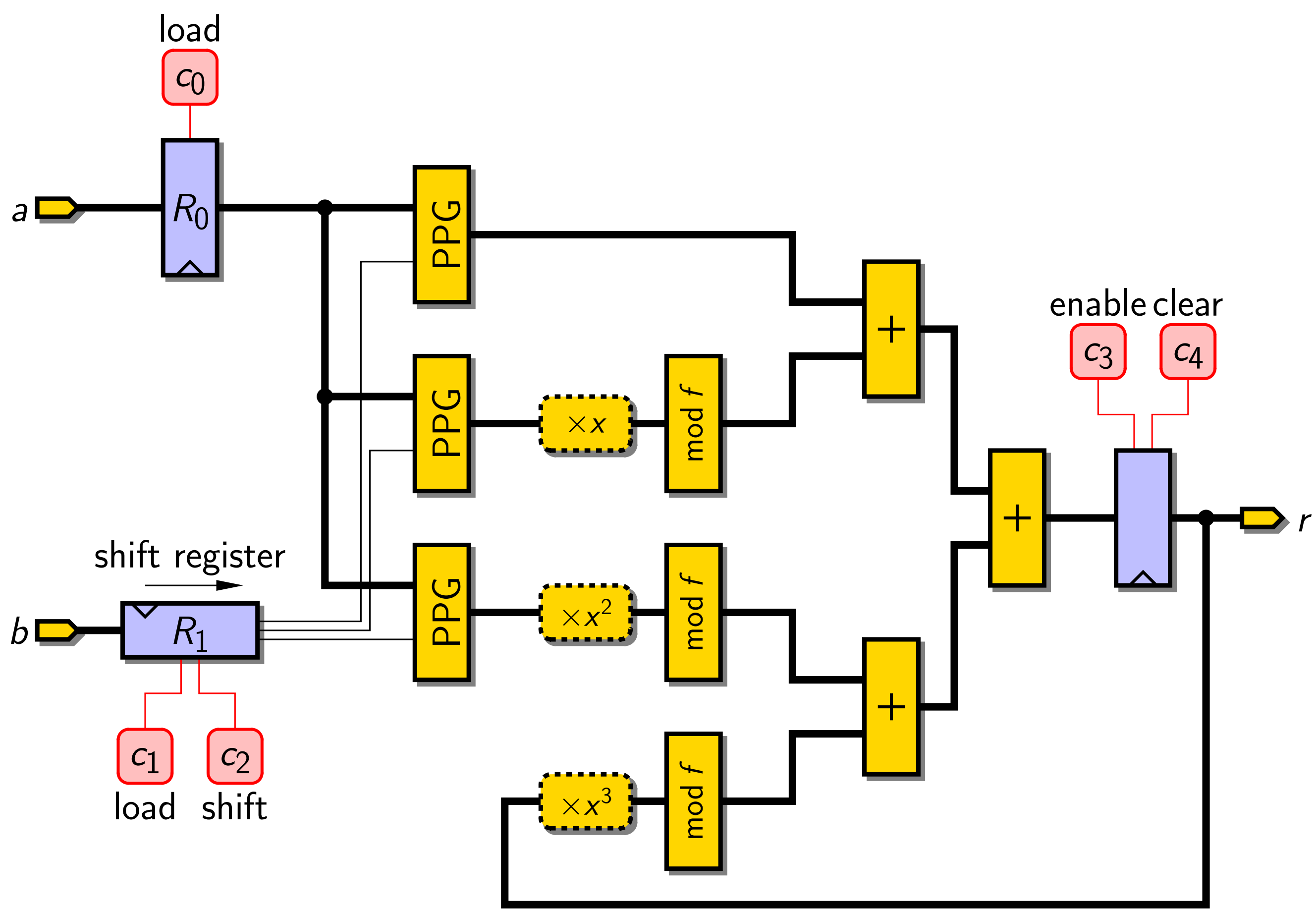

Frobenius map over $\mathbb{F}_{3^m}$: cubing

- Since $\binom{3}{1} = \binom{3}{2} = 3$:

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- Symbolic computation of the reduction:
  each coefficient of the result is a linear combination of the a_i's

$$a^3 \bmod f = \sum_{j=0}^{n-1} w_j \cdot \mu_j$$

with $w_j \in \mathbb{F}_3$, $\mu_j \in \mathbb{F}_{3^m}$, and $\mu_{j,i} \in \{0\} \cup \{a_{m-1}, \ldots, a_1, a_0\}$

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- Example for $m = 97$ and $f = x^{97} + x^{12} + 2$:

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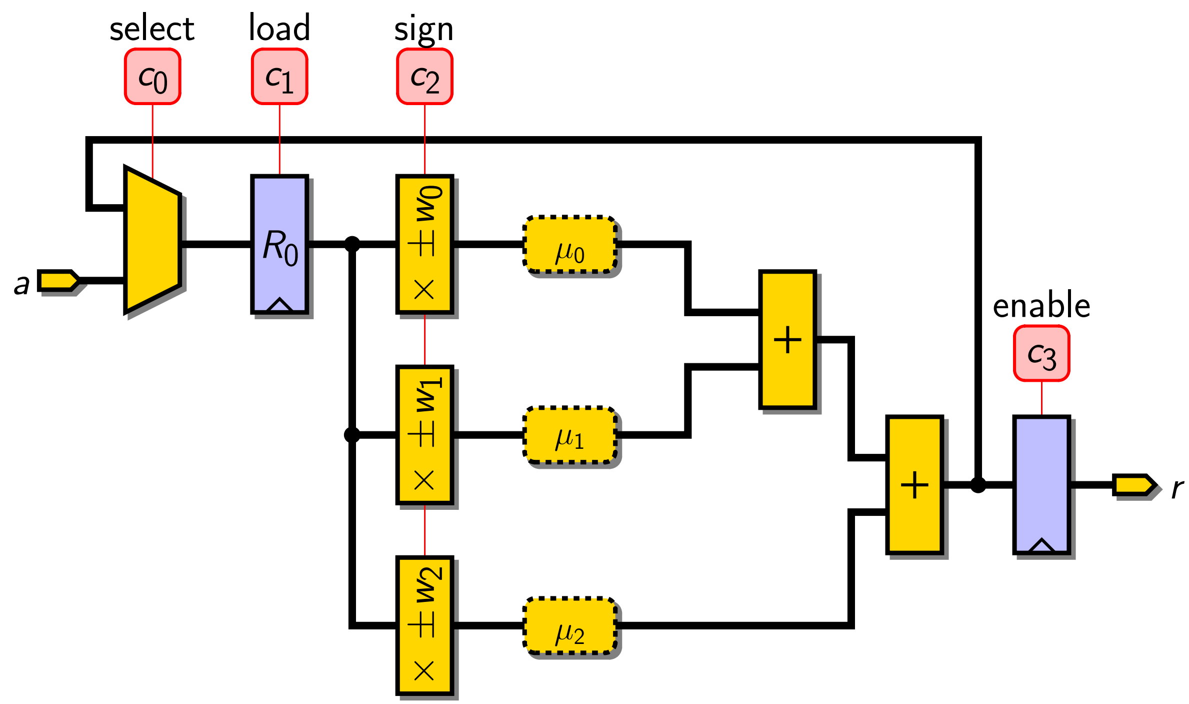
- Required hardware:
  - only wires to compute the μ_j's
  - multiplications over $\mathbb{F}_3$ for the weights w_j
  - multi-operand addition over $\mathbb{F}_{3^m}$

Frobenius map over $\mathbb{F}_{3^m}$



- feedback loop for successive cubings
- sign selection for computing either a^3 or $-a^3$

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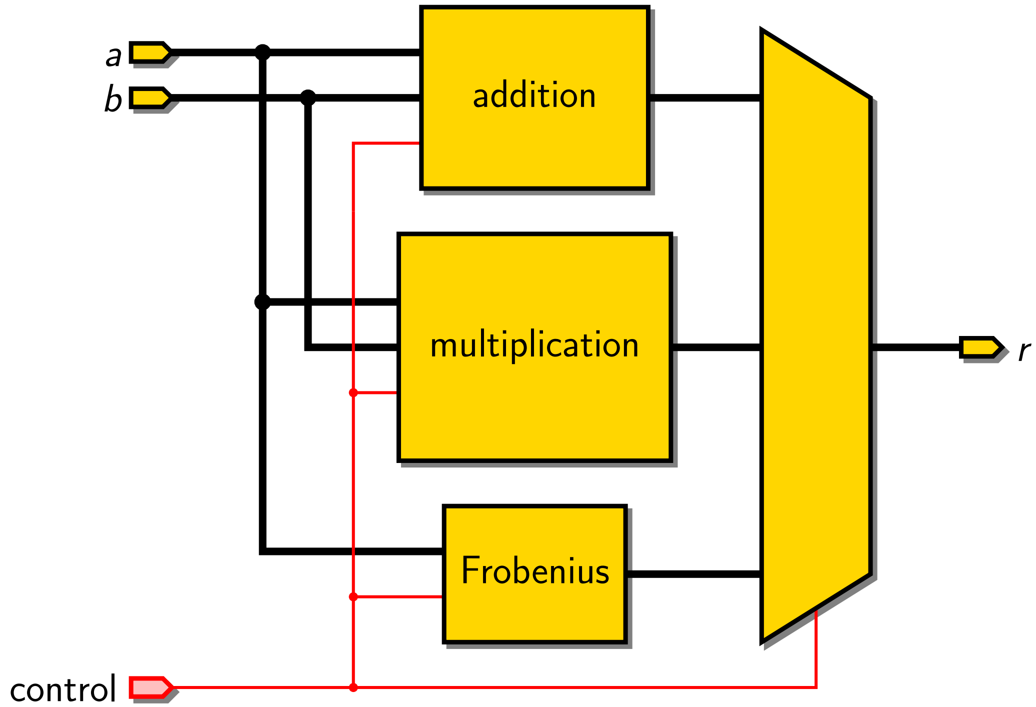
  - only one inversion for the full pairing: delay overhead is negligible ($< 1\%$)

The full processing element



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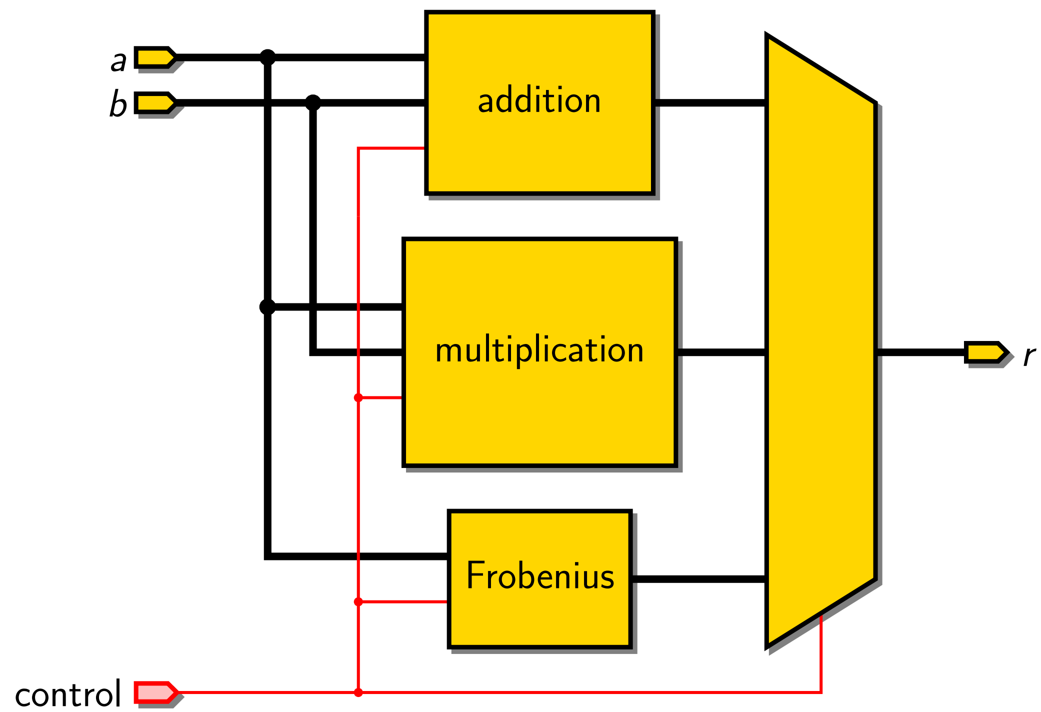


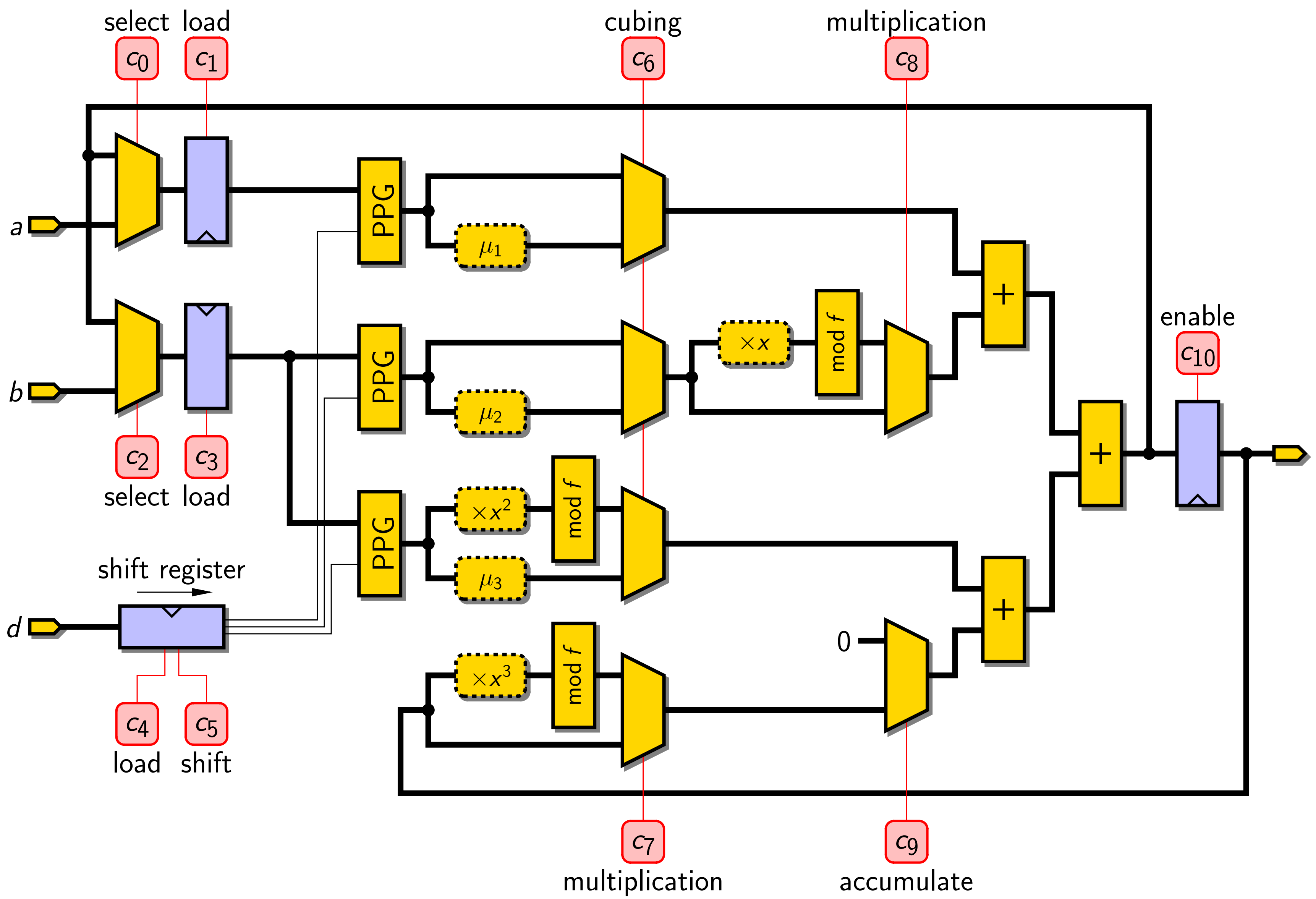
- For the Tate pairing:
  limited parallelism between additions, multiplications and Frobenius maps

- Can we share hardware resources between the three operators?

What can we share?

- Input and output registers
- Partial product generators:
  - sign selection for the addition / subtraction
  - partial products for the multiplication
  - multiplication by the w_j's for the Frobenius map
- Multi-operand addition tree
- Feedback loops for accumulation

Our unified operator



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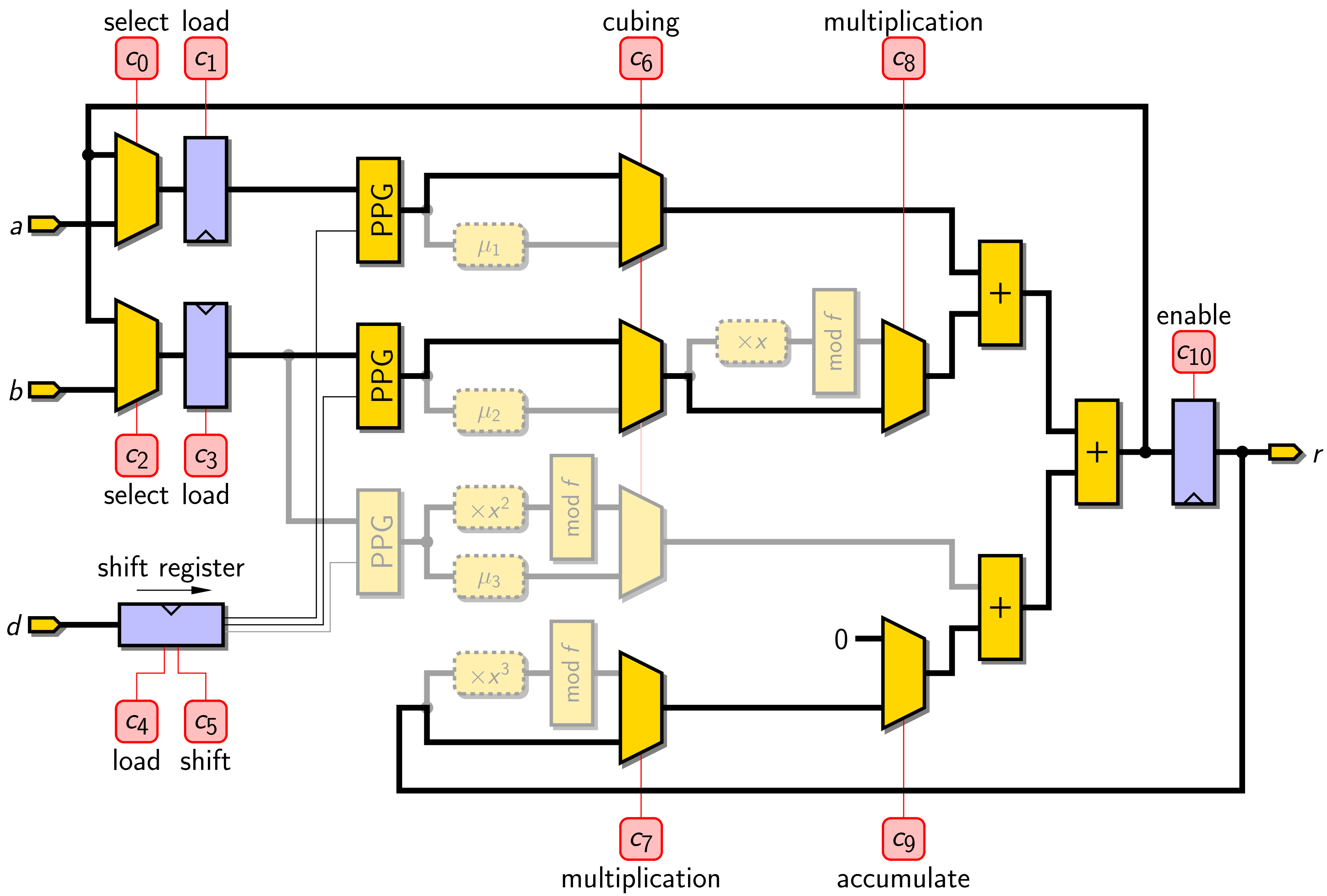

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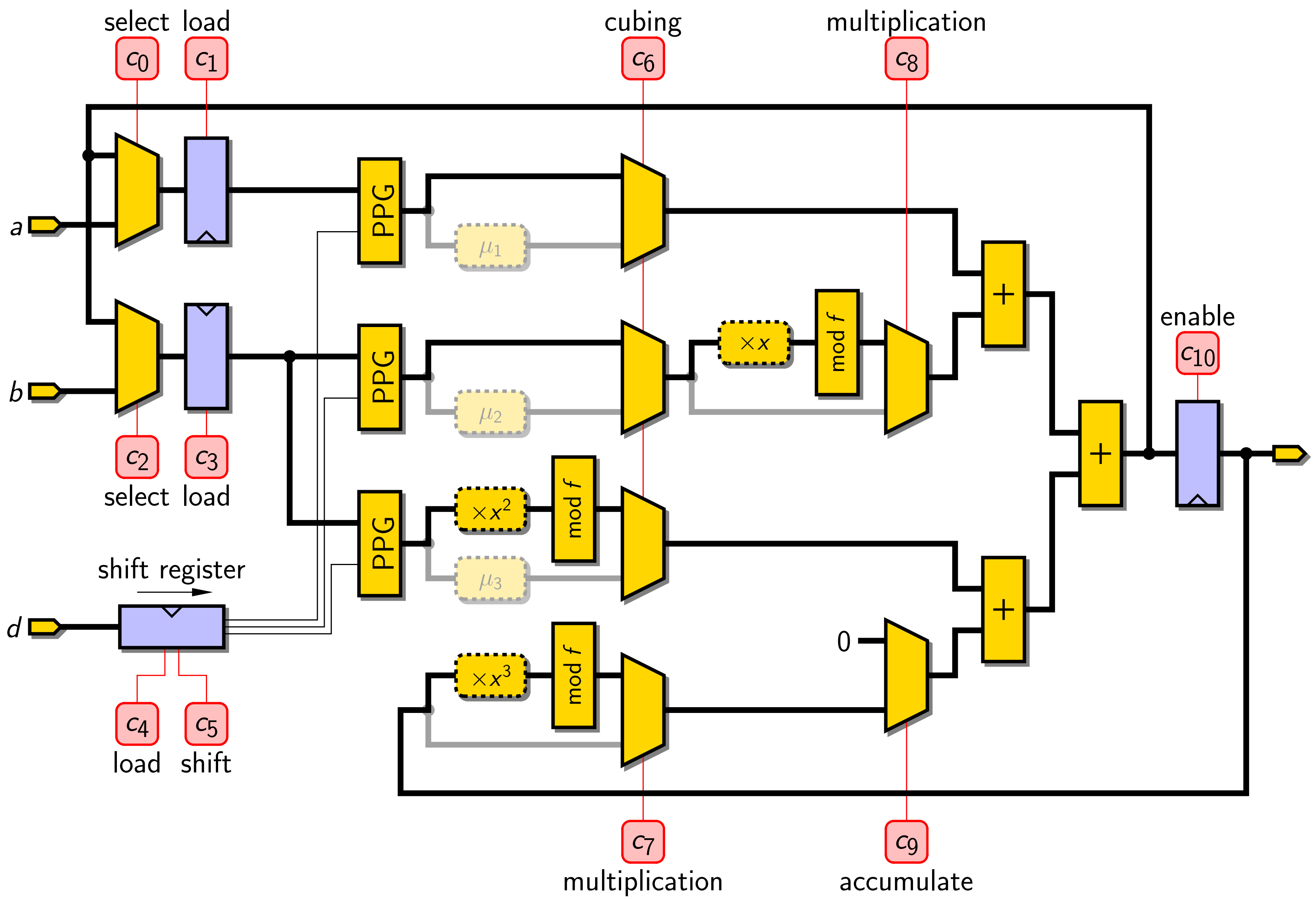

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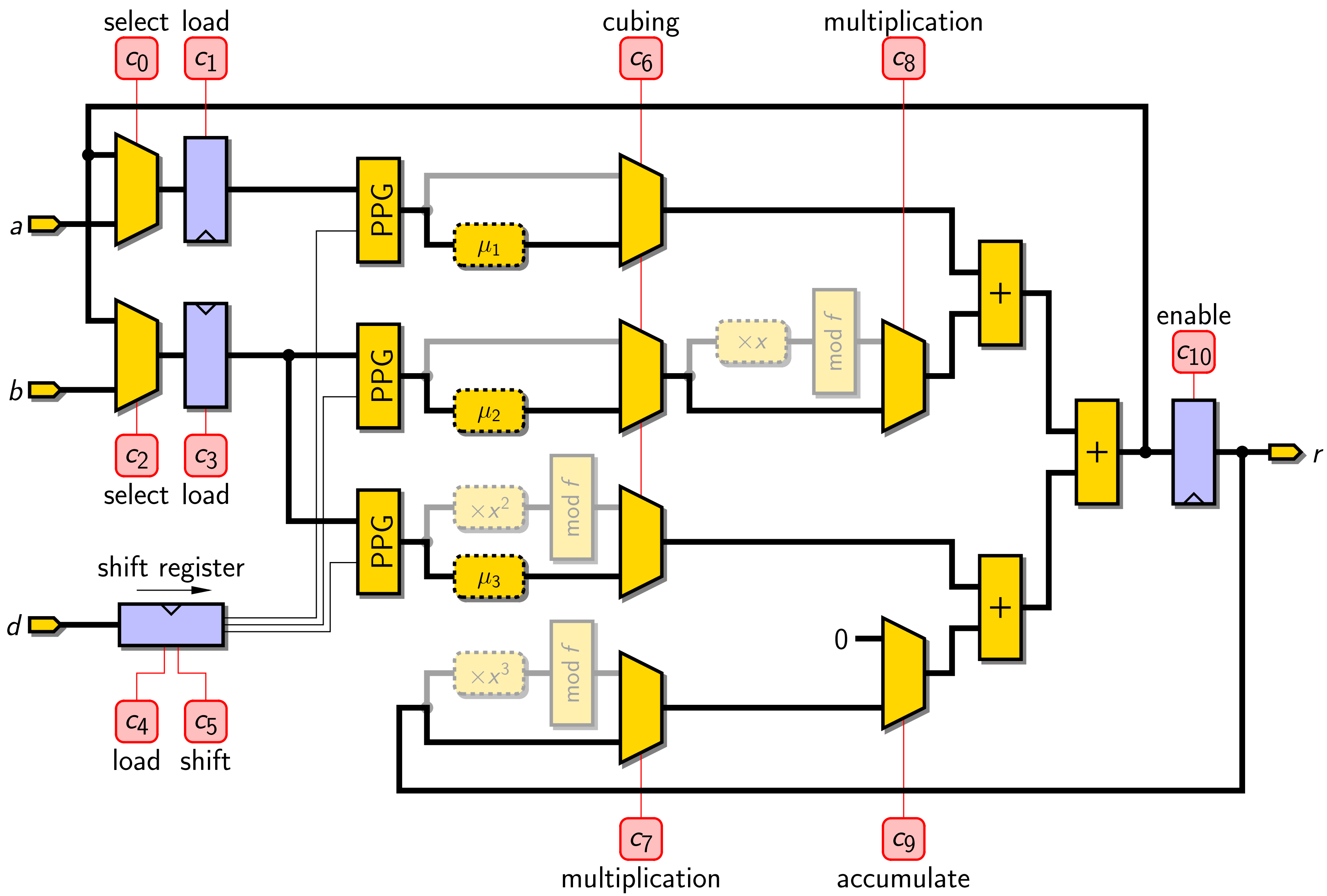


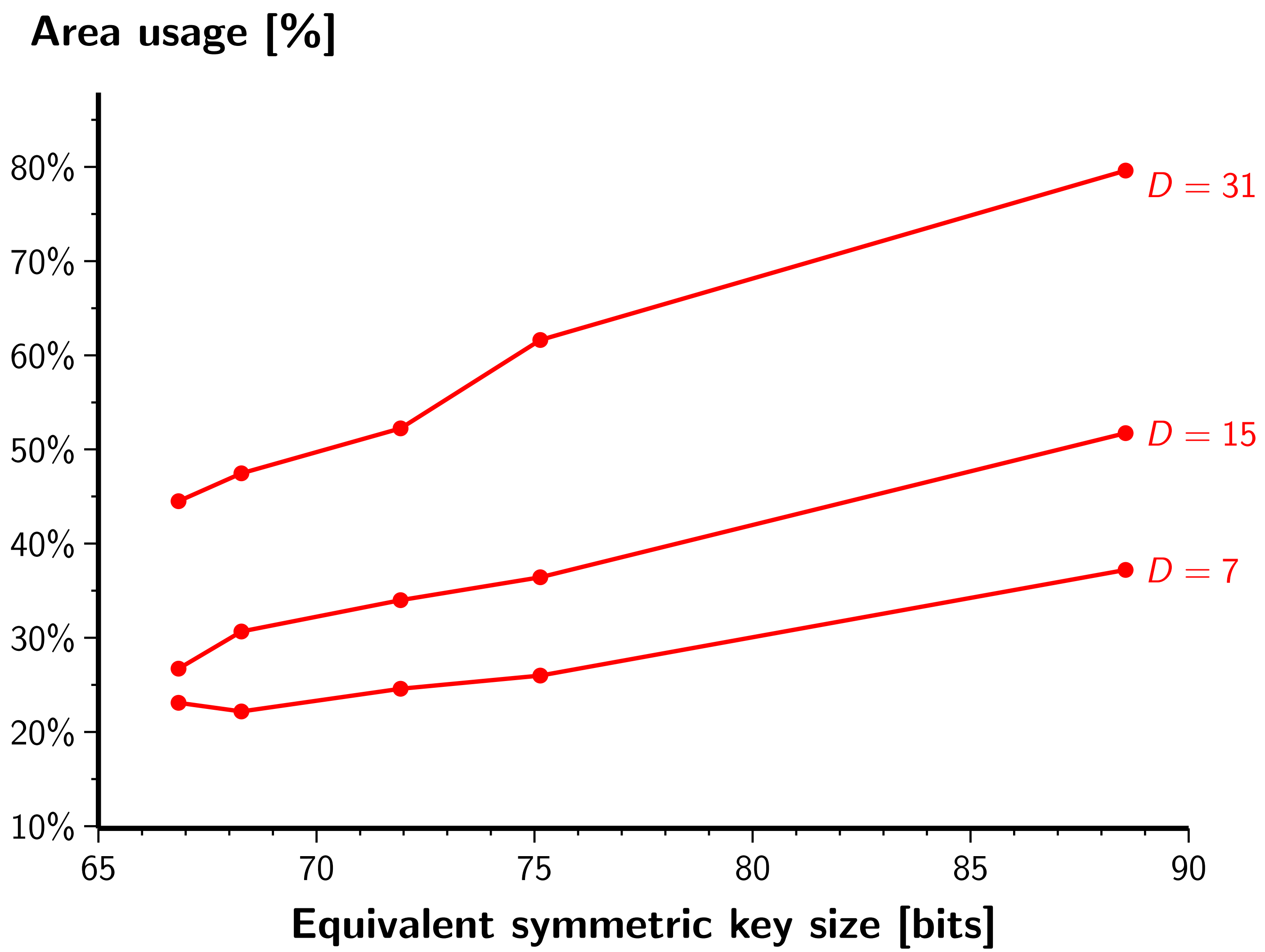
Outline of the talk

- Pairing-based cryptography
- Pairings over elliptic curves
- Finite-field arithmetic
- Implementation results
- Concluding thoughts

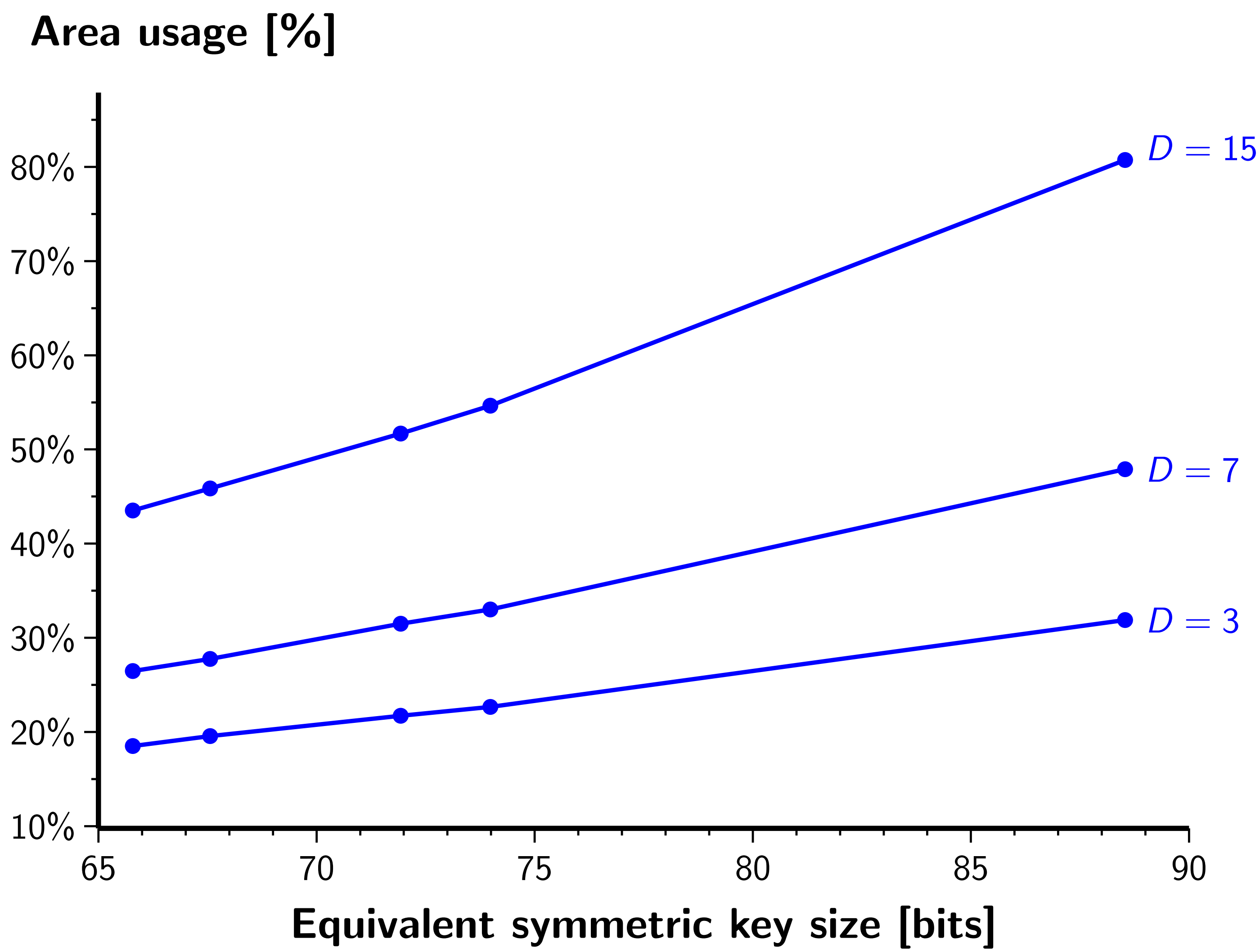
Experimental setup

- Full coprocessor for computation of the Tate pairing
- Architecture based on our unified operator
- Prototyped on a Xilinx Virtex-II Pro 20 FPGA (mid-range model)
- Post place-and-route results: area, computation time, AT product

Coprocessor area (characteristic 2)



Coprocessor area (characteristic 3)



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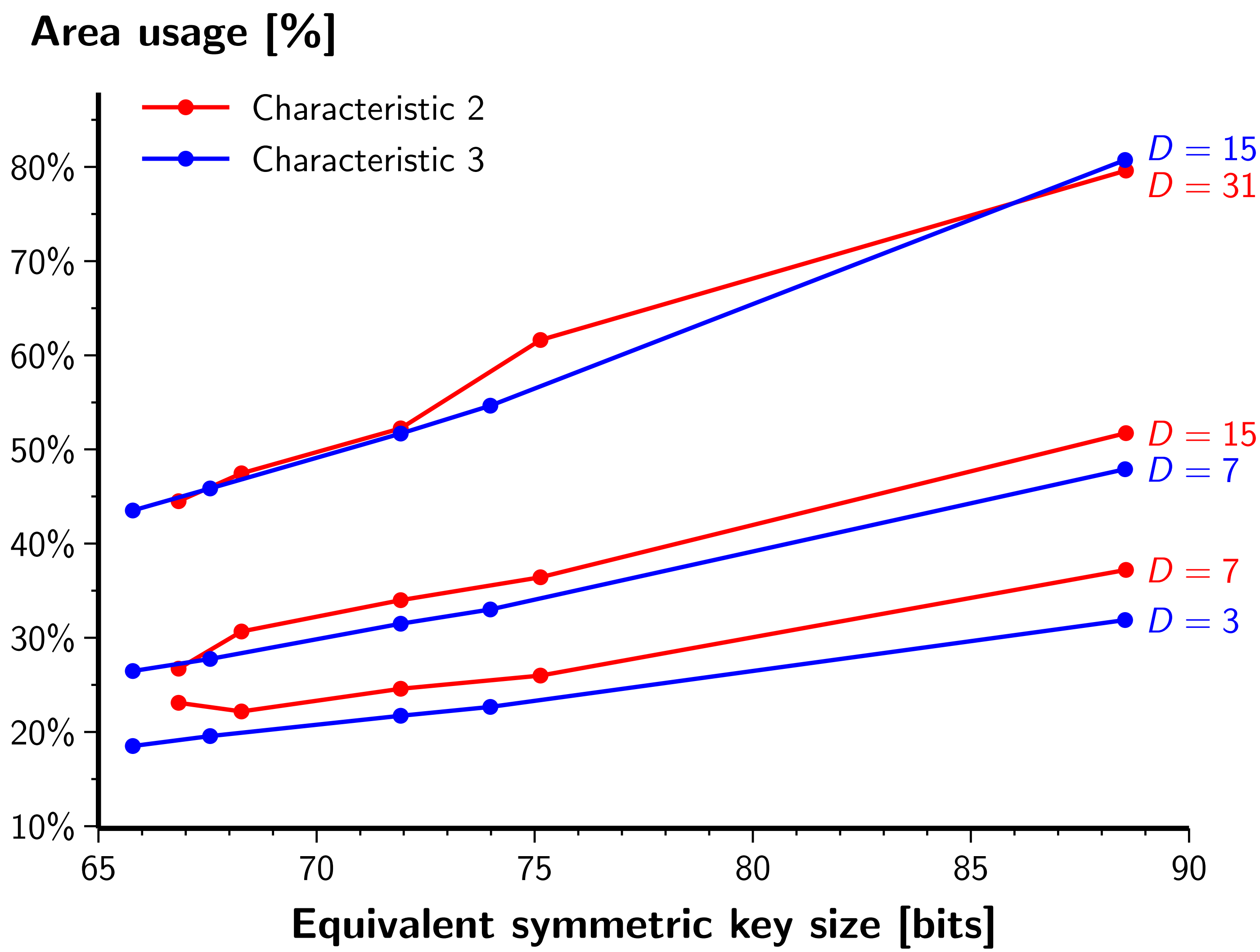
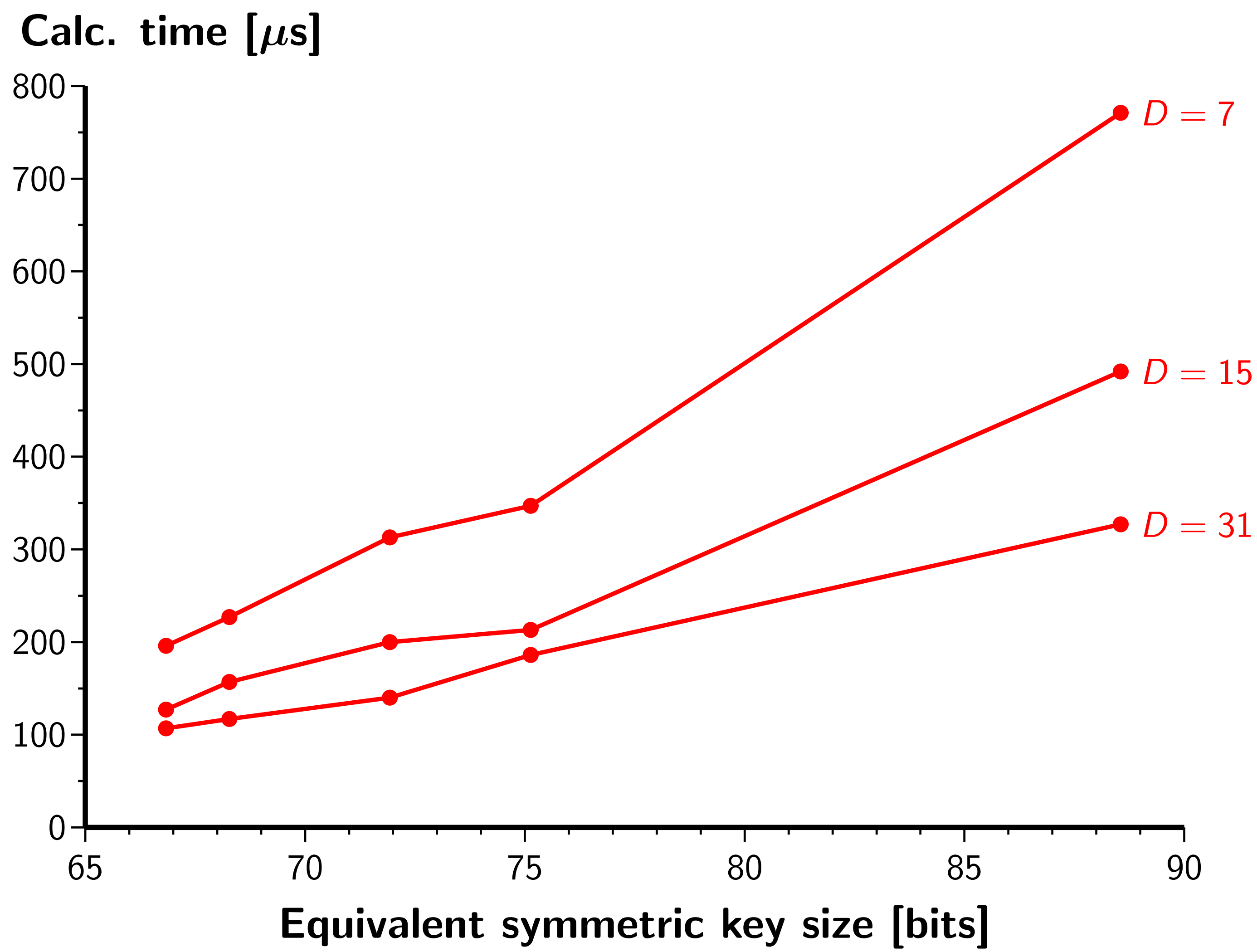


Calculation time (characteristic 2)



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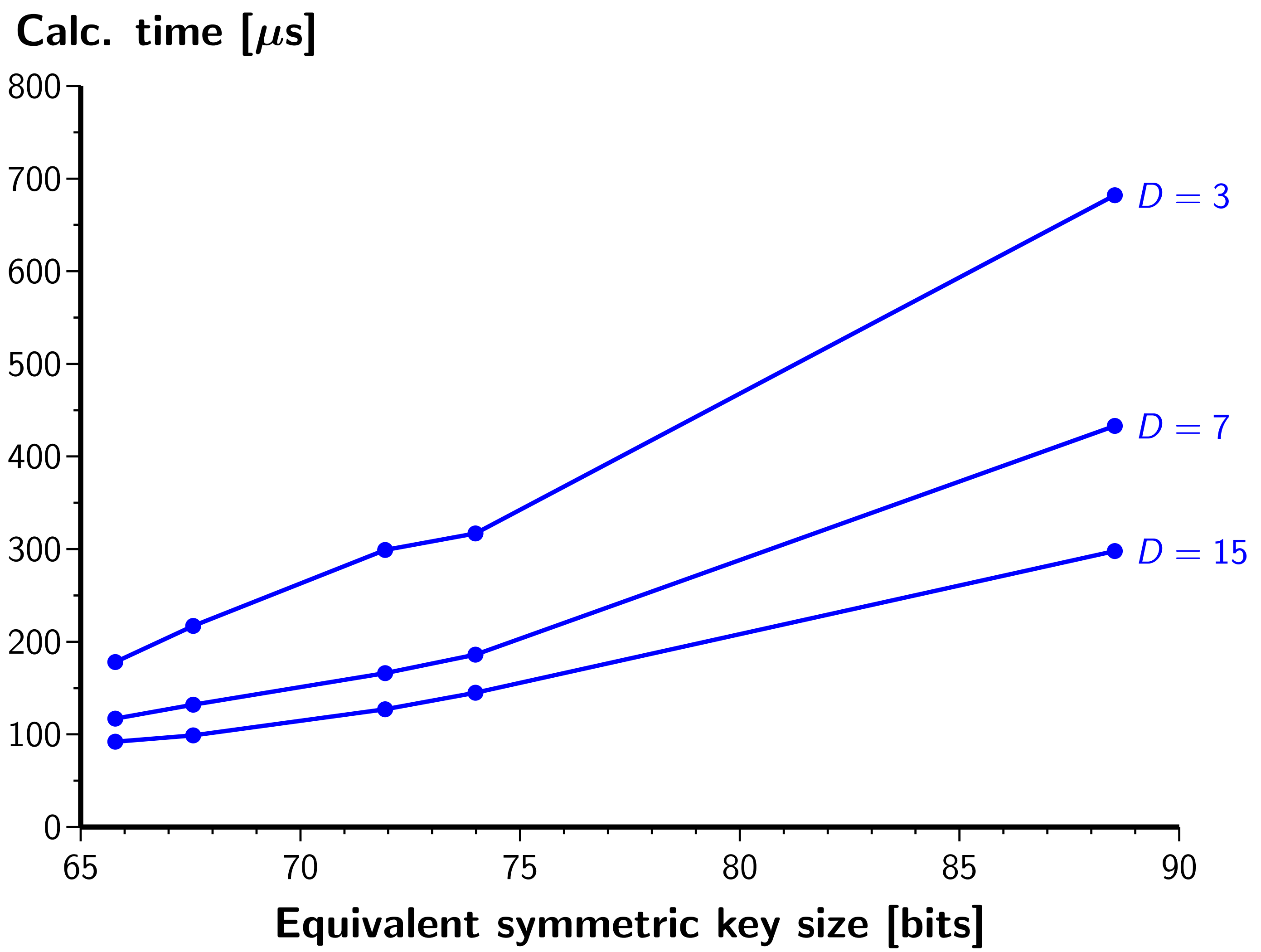

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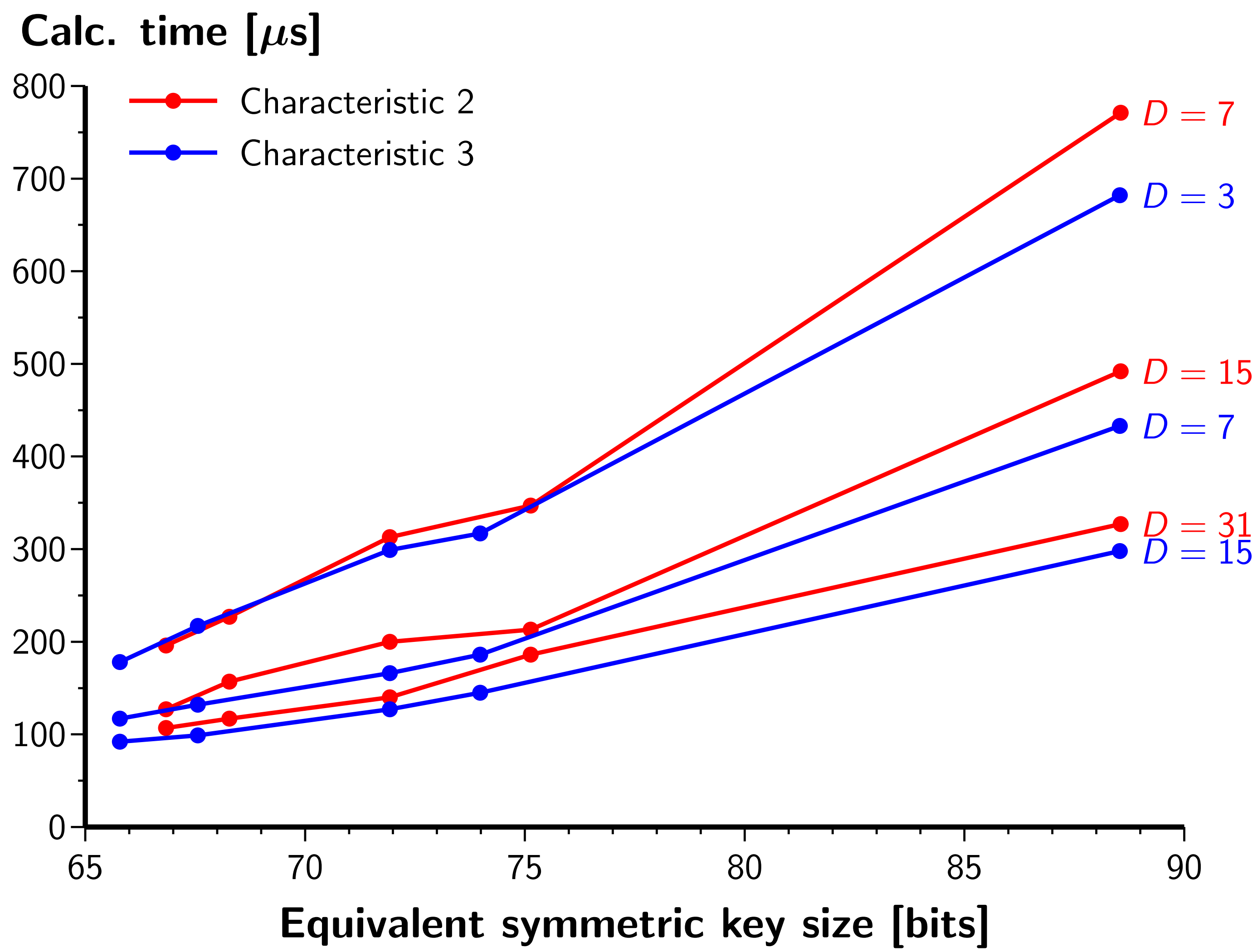

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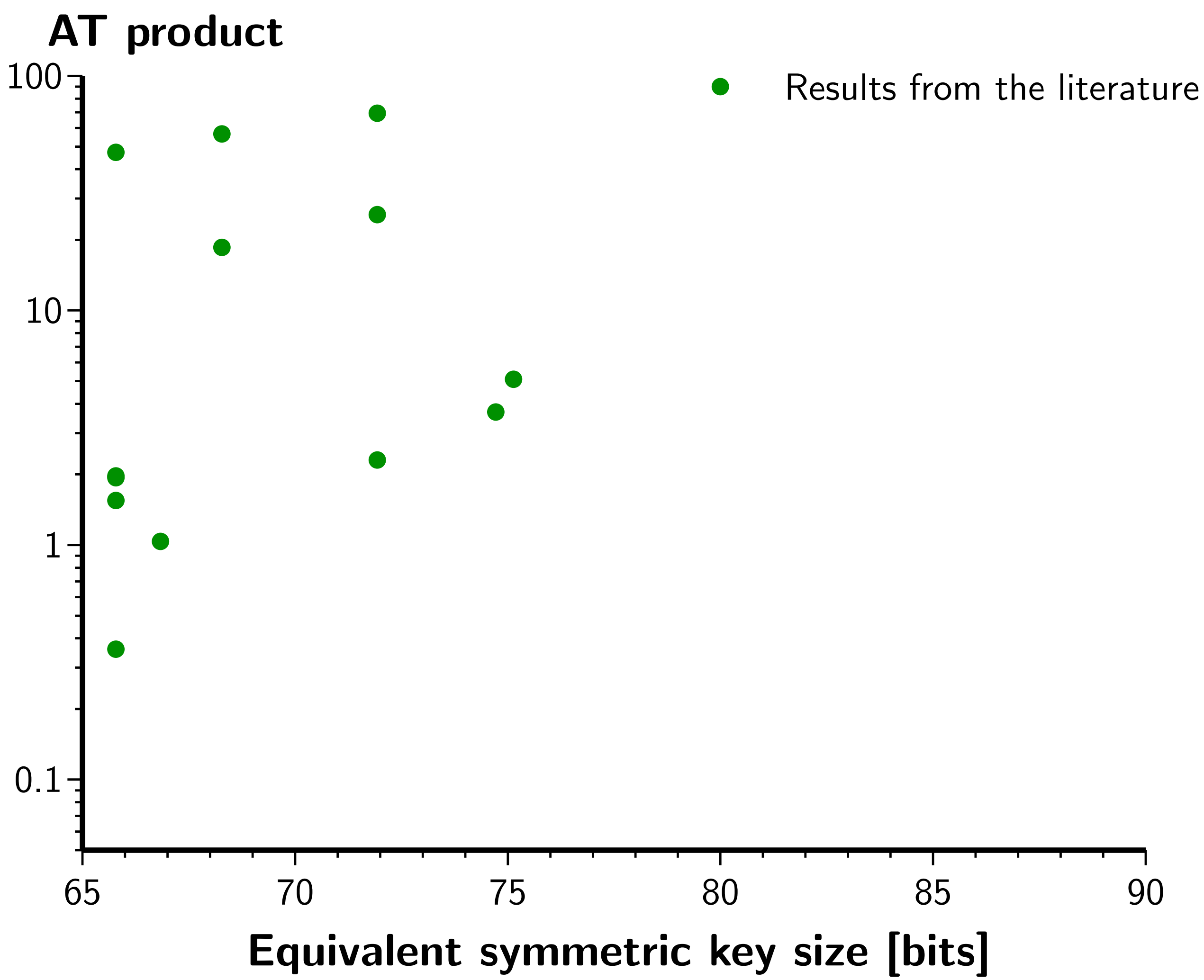

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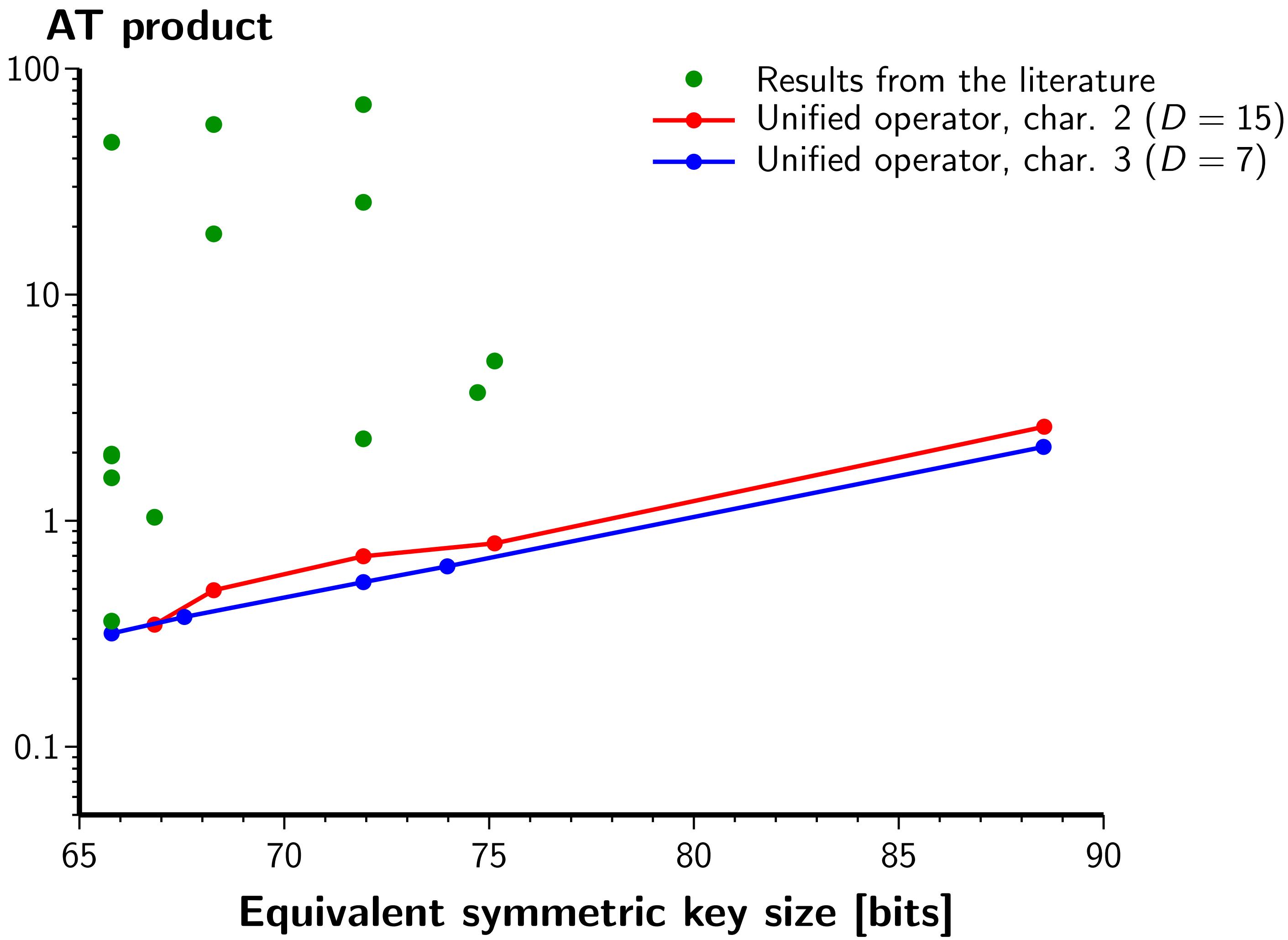

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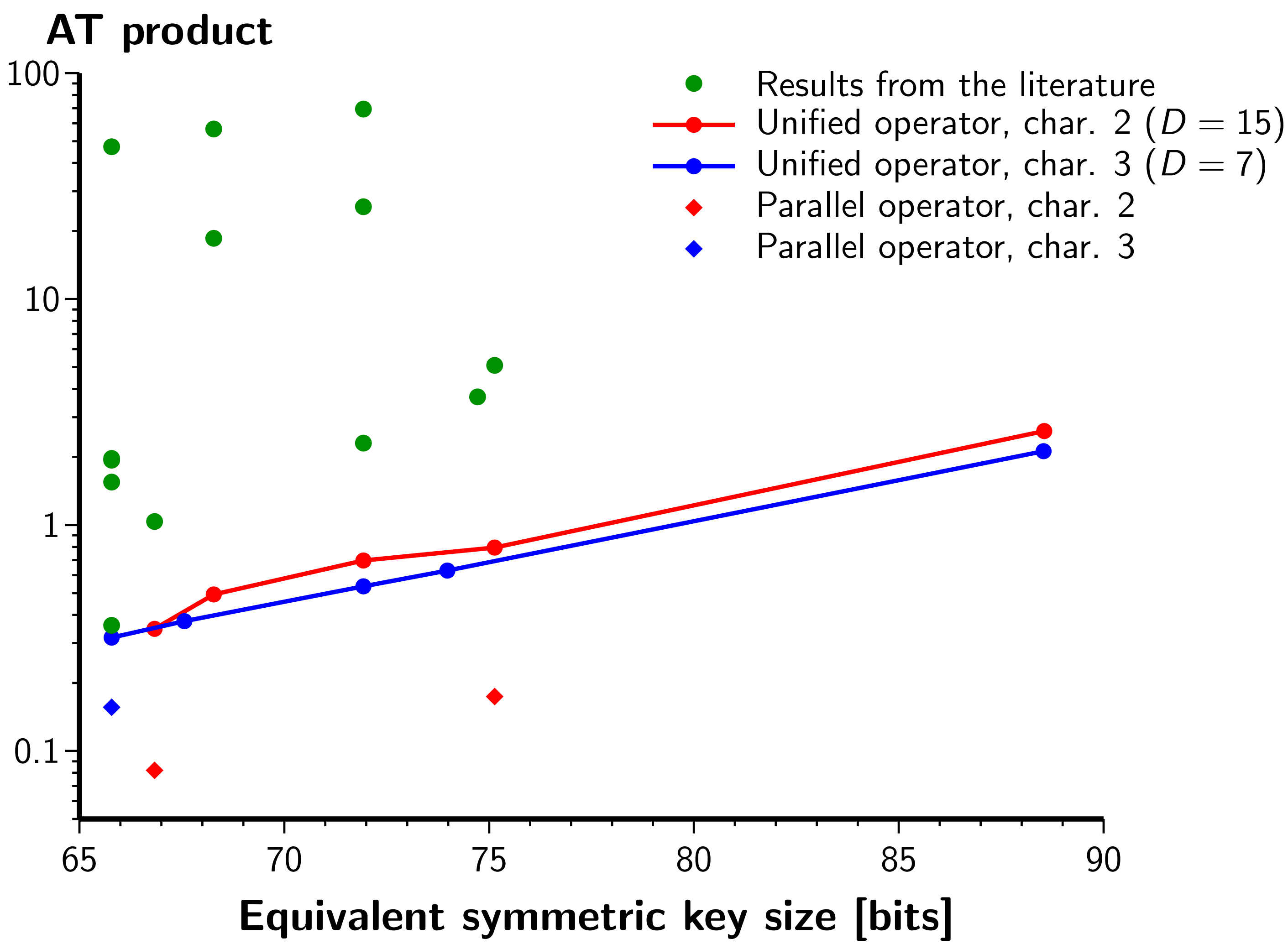

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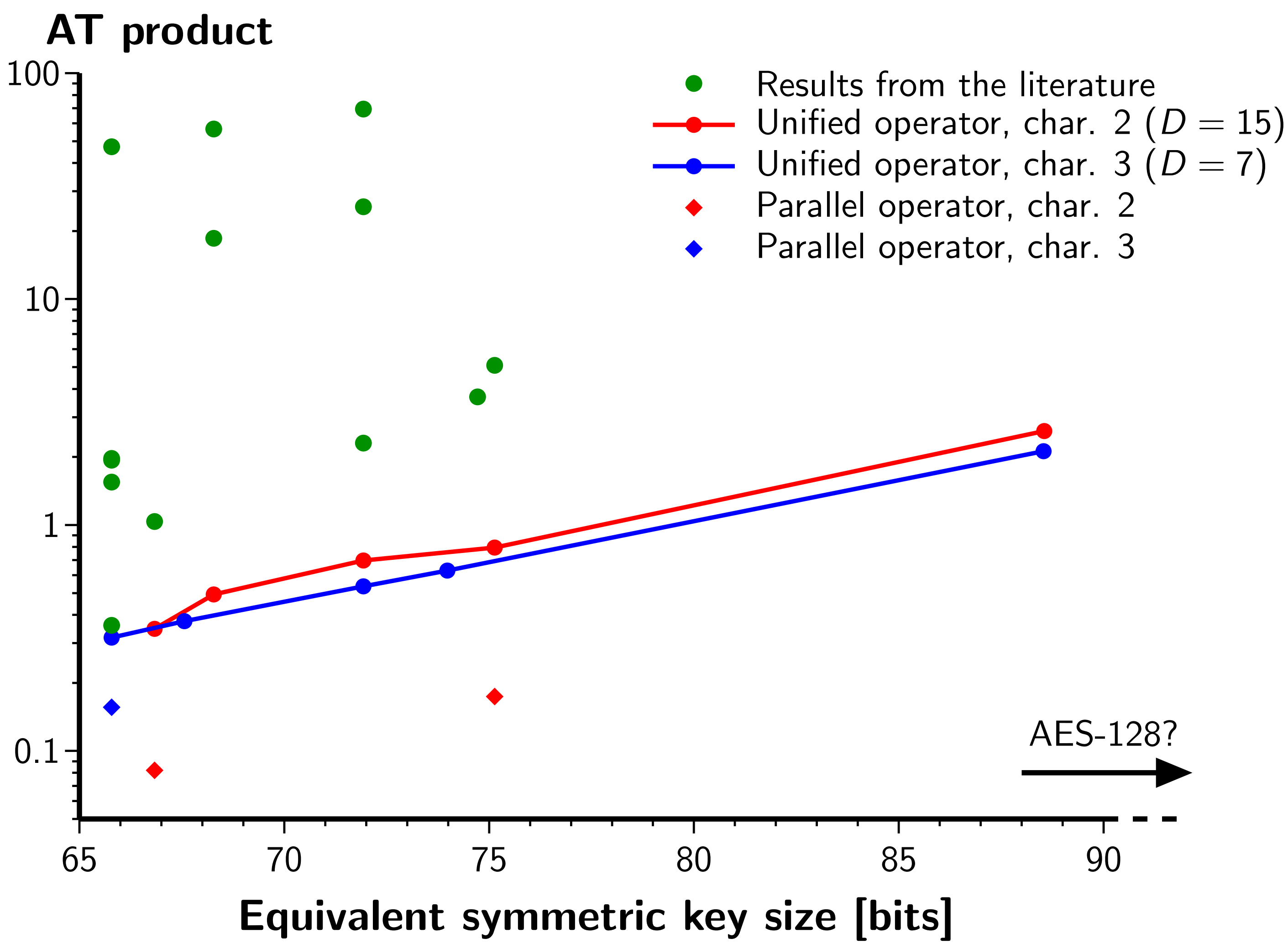

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With thanks to our sponsor

Thank you for your attention

Questions?